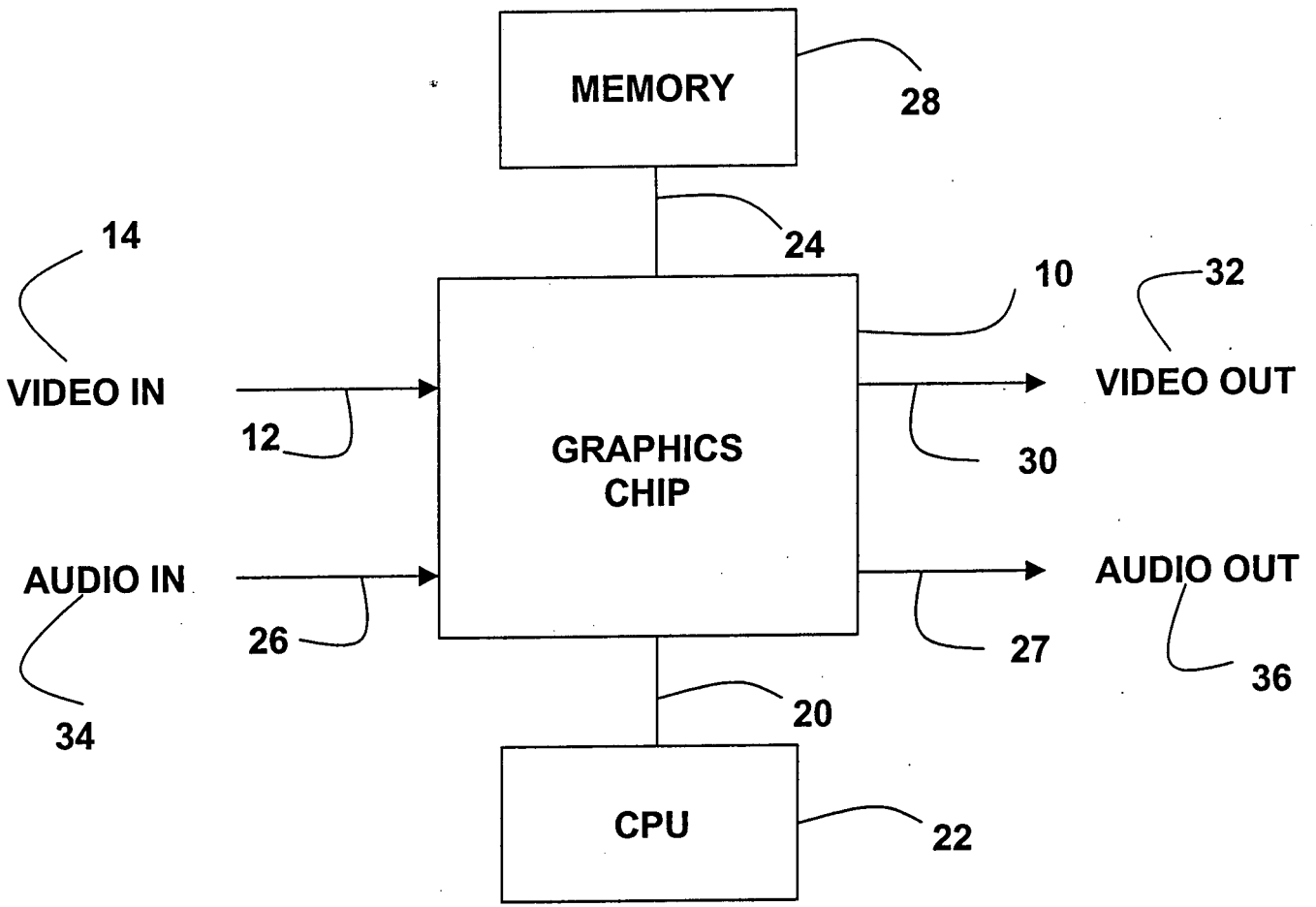

FIG. 1

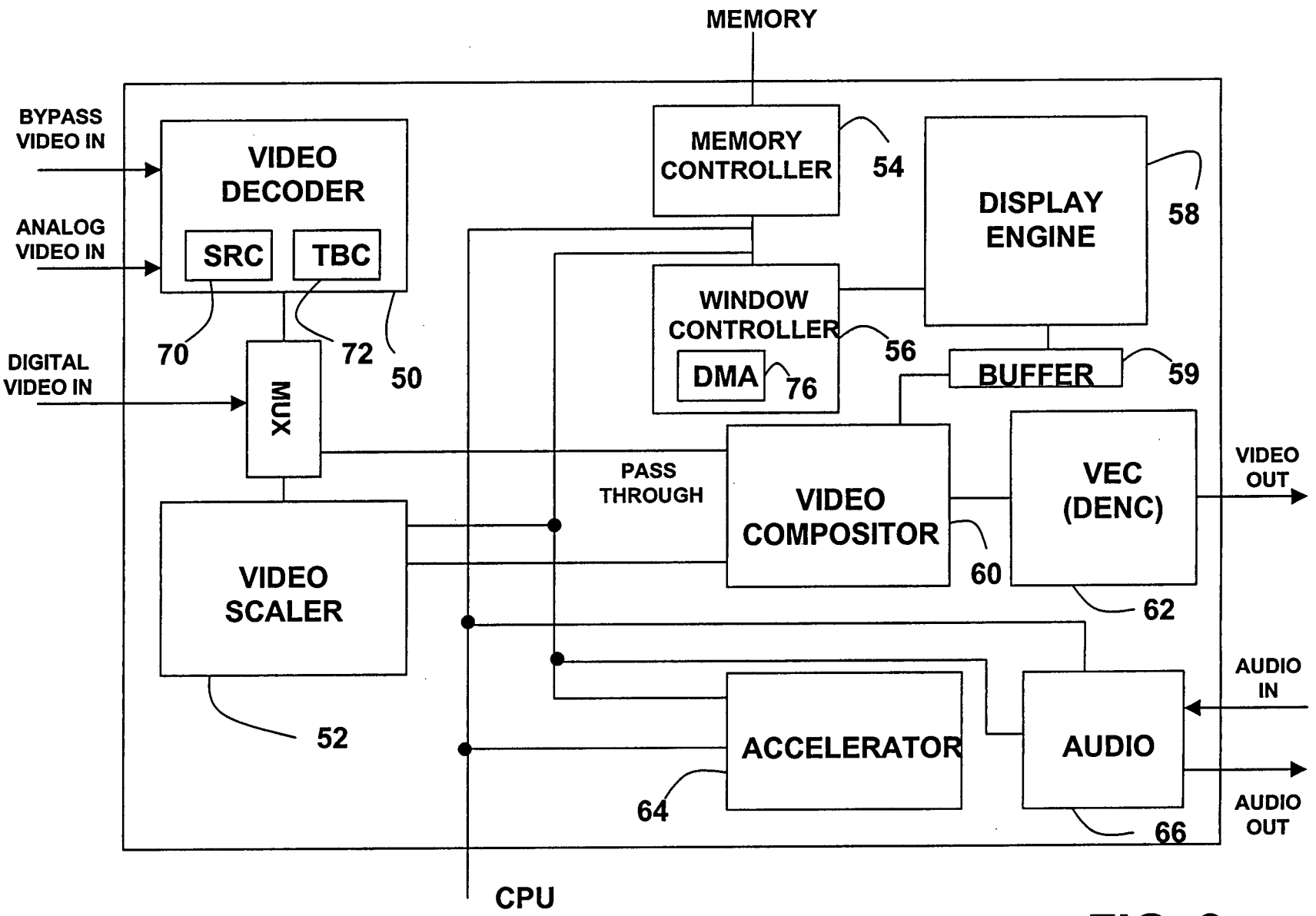

FIG. 2

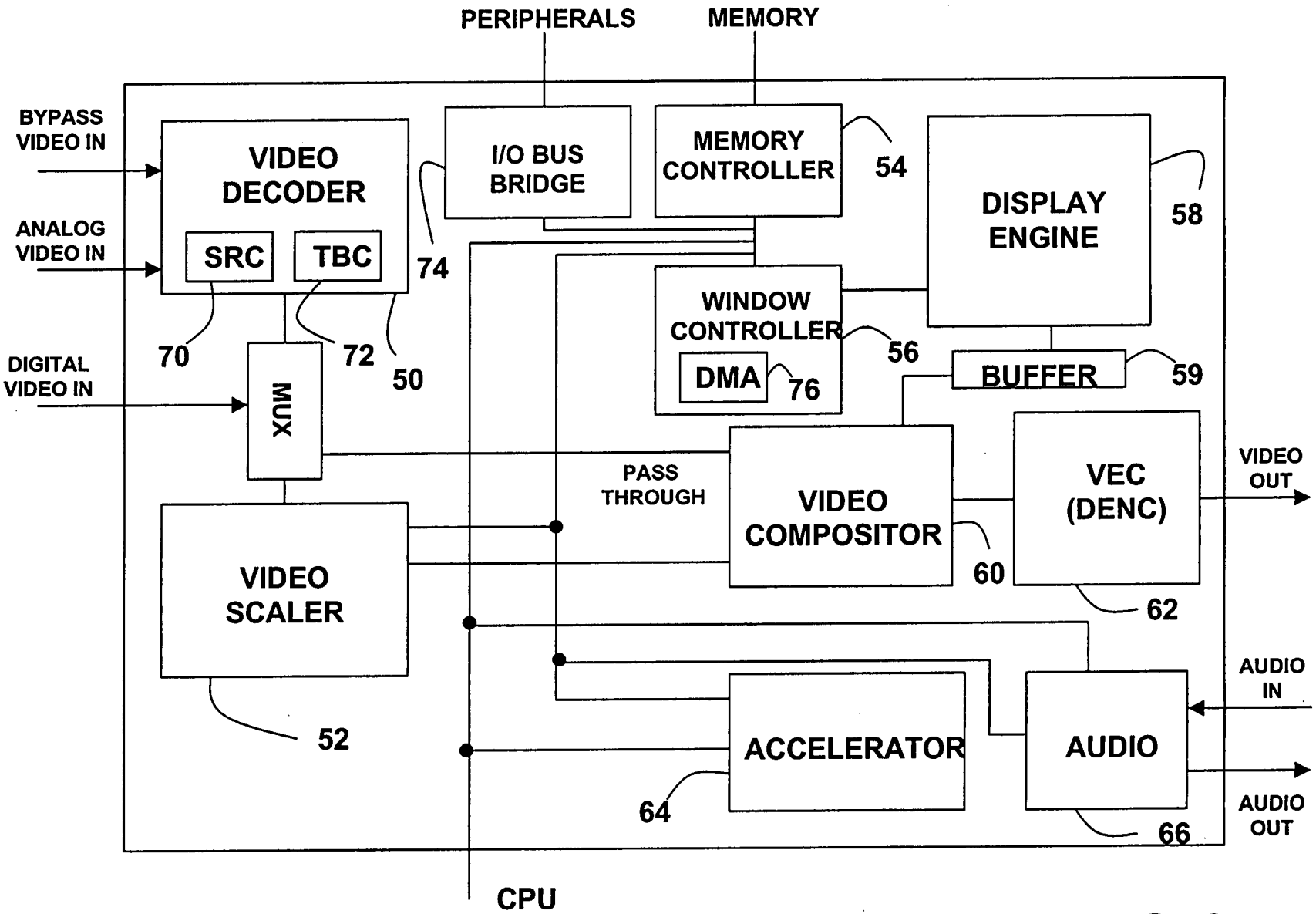

FIG. 3

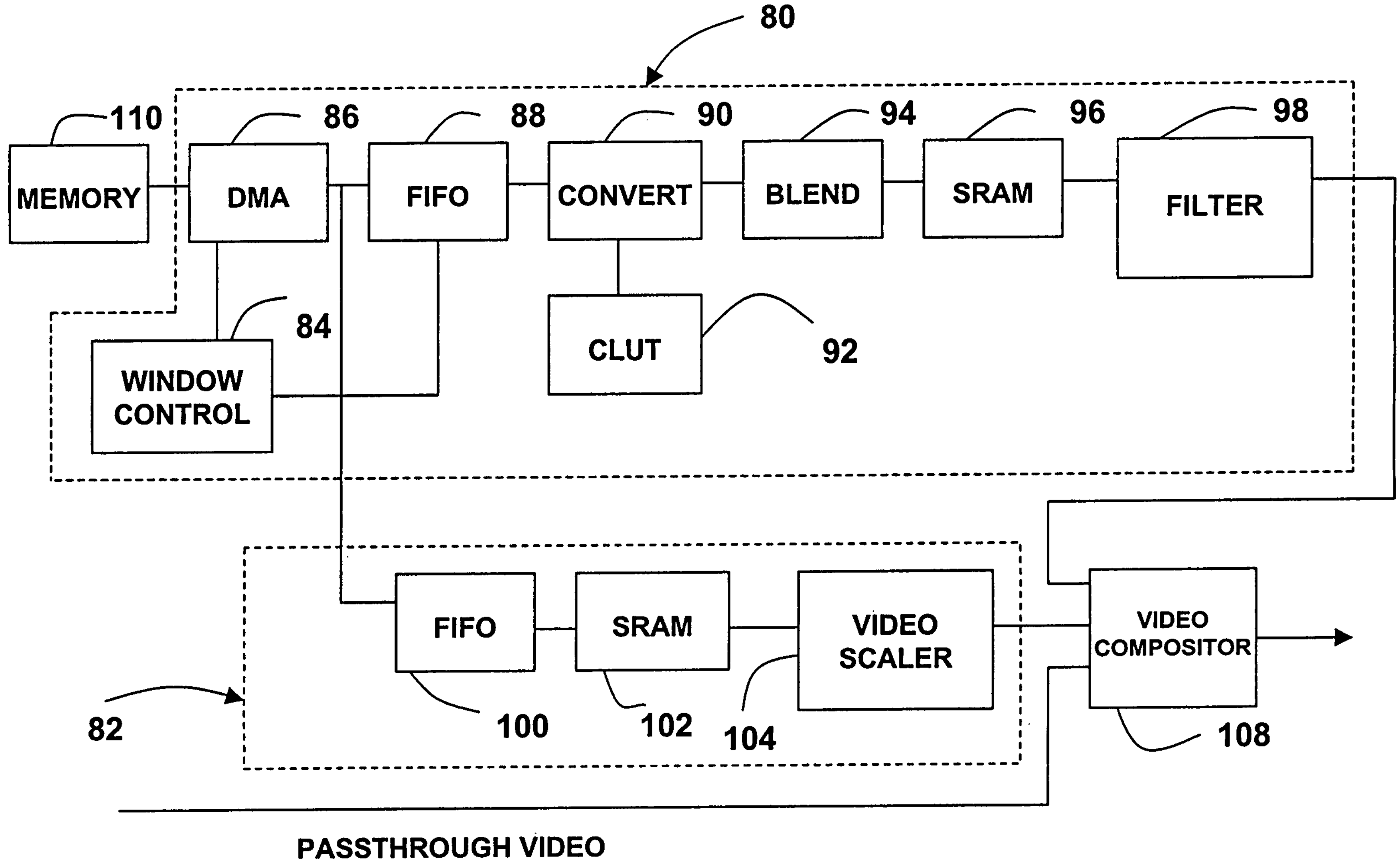
80
110
MEMORY
86
DMA
88
FIFO
90
CONVERT
94
BLEND
96
SRAM
98
FILTER
84
WINDOW CONTROL
CLUT
92
82
FIFO
SRAM
VIDEO SCALER
100
102
104
VIDEO COMPOSITOR
108
PASSTHROUGH VIDEO

FIG. 4

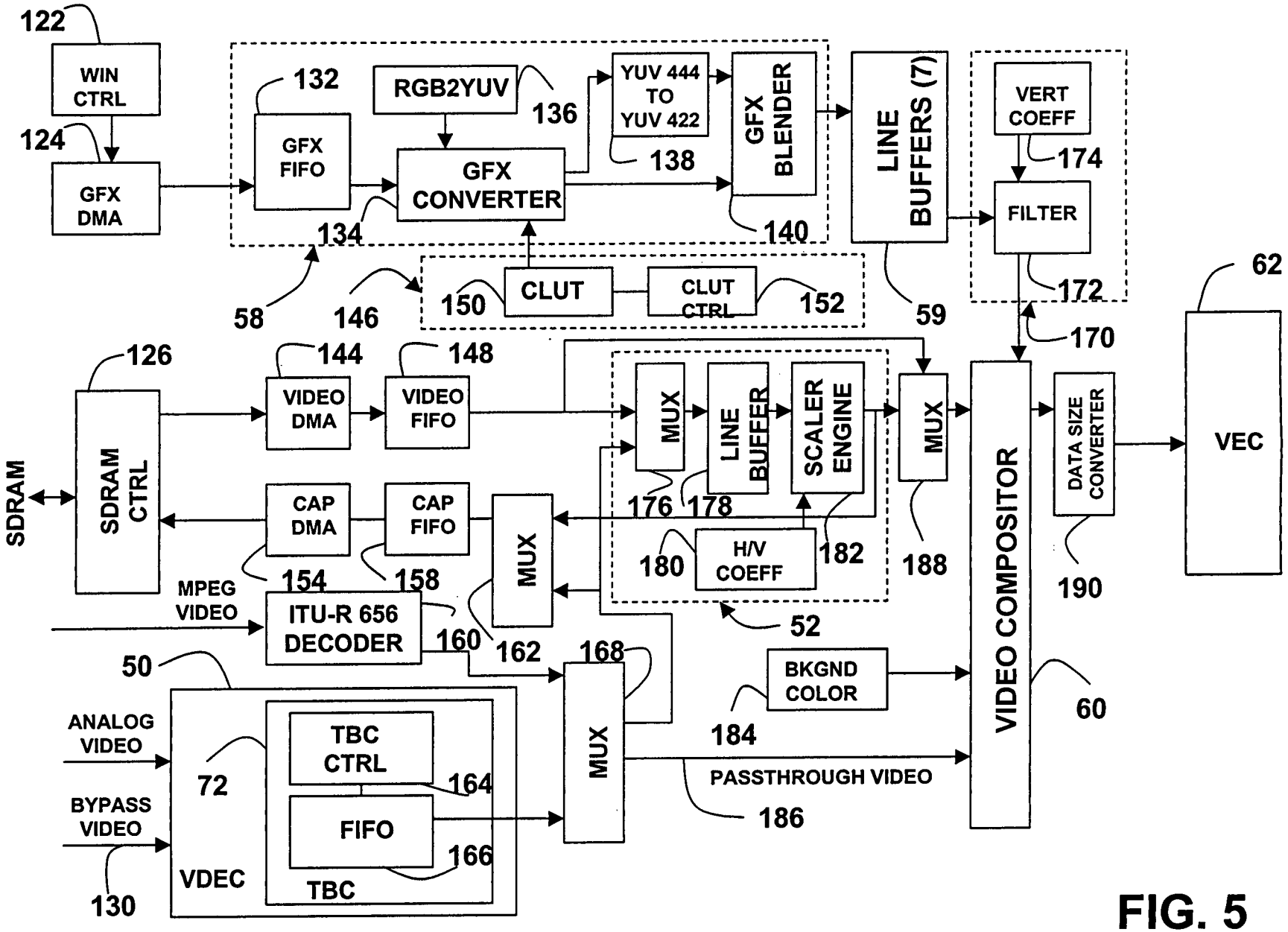
122
WIN CTRL
124
GFX DMA
132
GFX FIFO
RGB2YUV
136
GFX CONVERTER
YUV 444 TO YUV 422
138
GFX BLENDER
140
LINE BUFFERS (7)
VERT COEFF
174
FILTER
172
134
58
146
150
CLUT
CLUT CTRL
152
59
170
62
126
144
148
VIDEO DMA
VIDEO FIFO
MUX
LINE BUFFER
SCALER ENGINE
MUX
VIDEO COMPOSITOR
DATA SIZE CONVERTER
VEC
SDRAM
SDRAM CTRL
CAP DMA
CAP FIFO
MUX
176
178
H/V COEFF
180
182
188
190
MPEG VIDEO
154
158
ITU-R 656 DECODER
160
162
168
52
50
BKGND COLOR
184
60
ANALOG VIDEO
BYPASS VIDEO
72
TBC CTRL
164
FIFO
166
VDEC
TBC
130
MUX
PASSTHROUGH VIDEO
186

FIG. 5

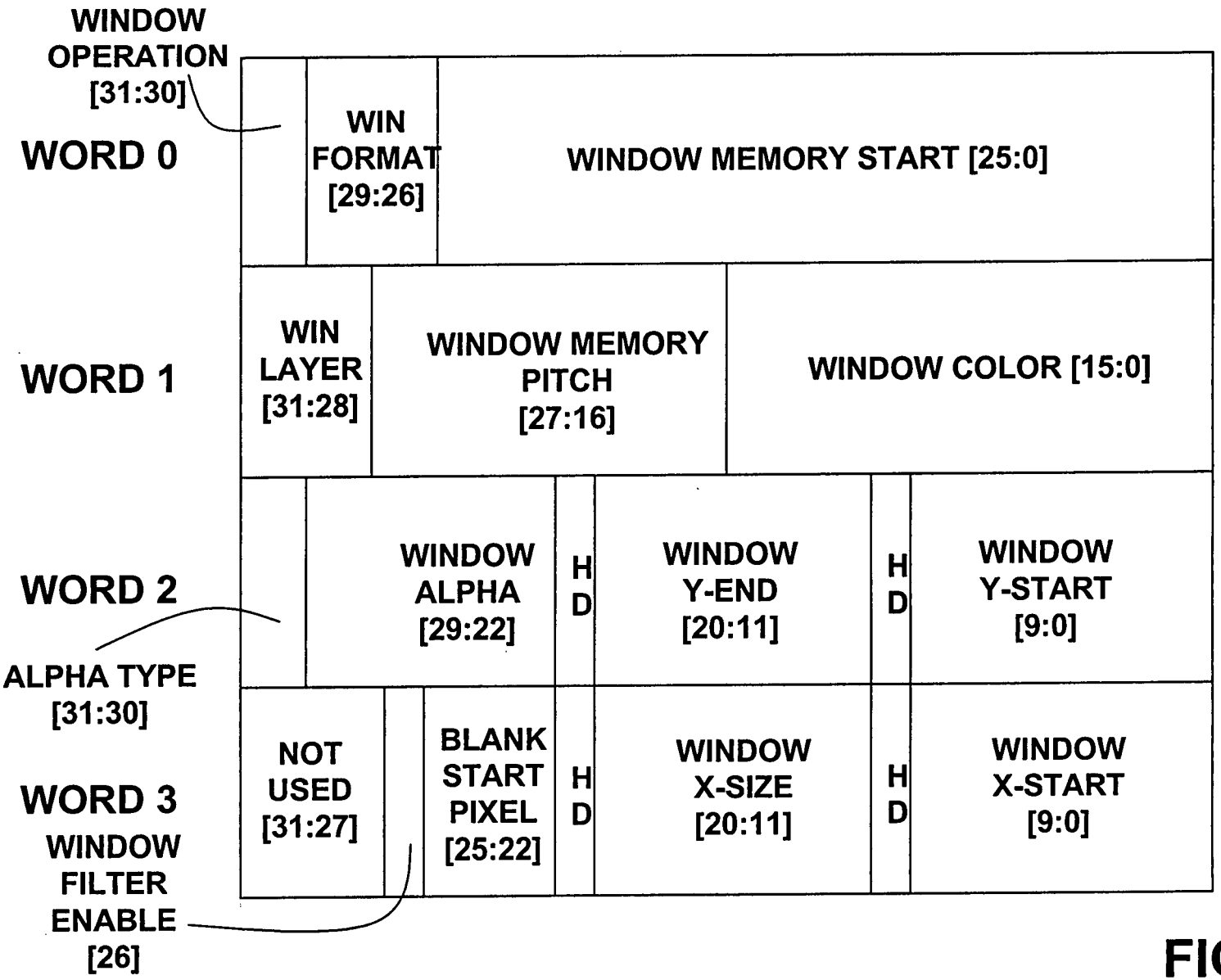

FIG. 6

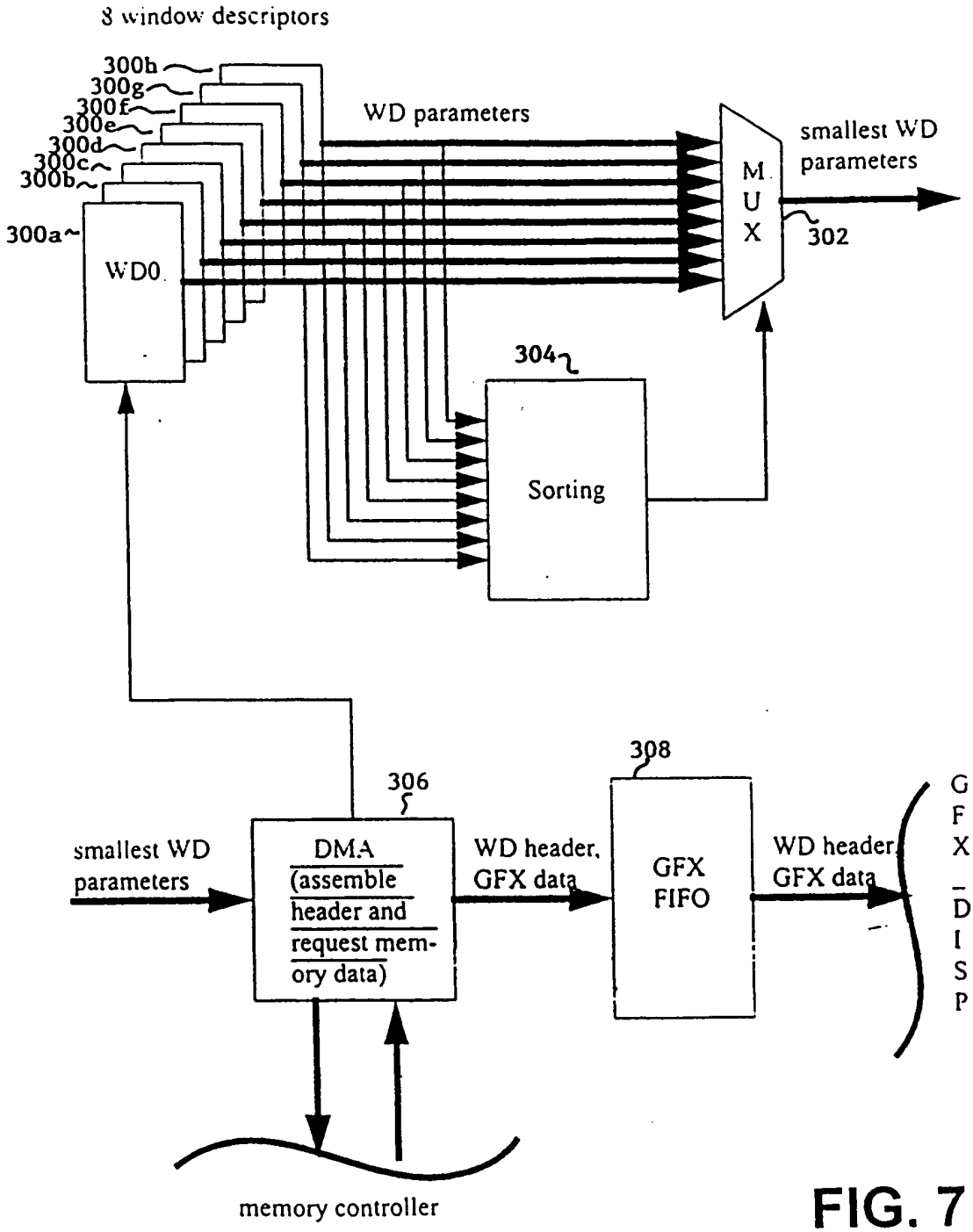
8 window descriptors
300h
300g
300f
300e
300d
300c
300b
300a
WD0
WD parameters
MUX
smallest WD parameters
302
304
Sorting
306
DMA (assemble header and request memory data)
smallest WD parameters
WD header, GFX data
308
GFX FIFO
WD header, GFX data
GFX_DISP
memory controller

FIG. 7

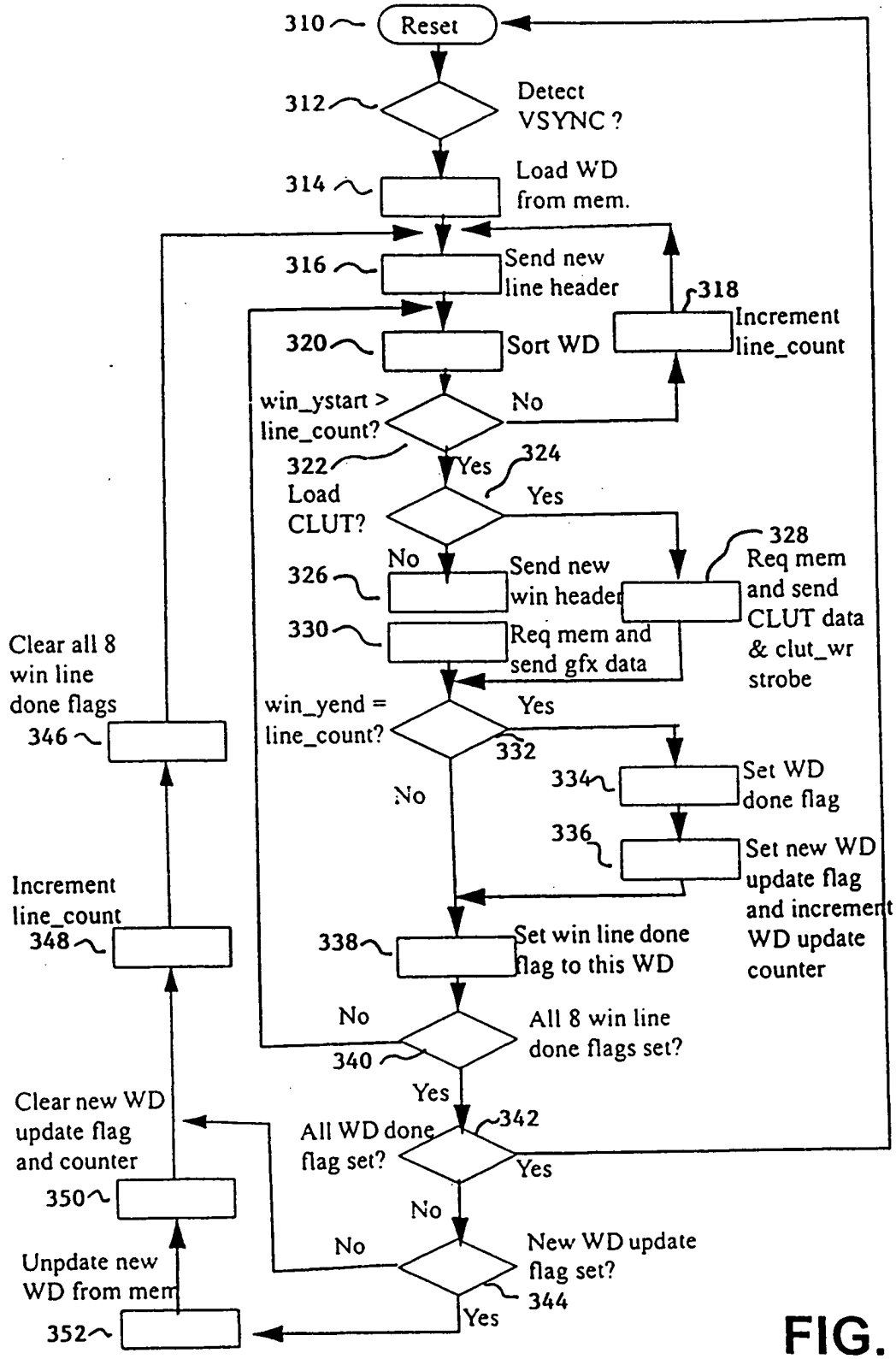
310
Reset
312
Detect VSYNC ?
314
Load WD from mem.
316
Send new line header
318
Increment line_count
320
Sort WD
win_ystart > line_count?
No
322
Load CLUT?
Yes
324
Yes
No
326
Send new win header
328
Req mem and send CLUT data & clut_wr strobe
330
Req mem and send gfx data
win_yend = line_count?
Yes
332
No
334
Set WD done flag
336
Set new WD update flag and increment WD update counter
338
Set win line done flag to this WD
No
All 8 win line done flags set?
340
Yes
342
All WD done flag set?
Yes
No
No
New WD update flag set?
344
Yes
Clear all 8 win line done flags
346
Increment line_count
348
Clear new WD update flag and counter
350
Unpdate new WD from mem
352

FIG. 8

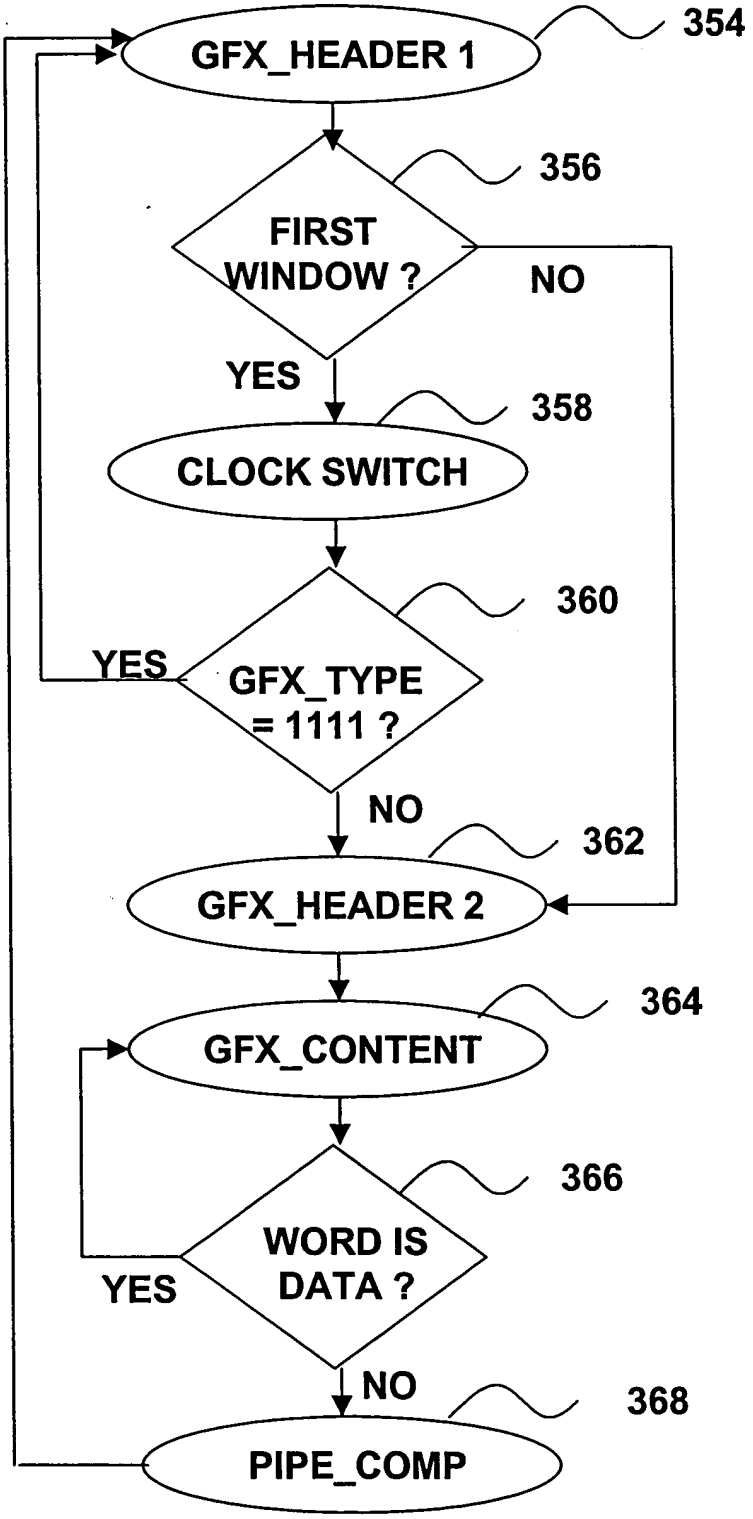
GFX_HEADER 1
354
356
FIRST WINDOW ?
NO
YES
358
CLOCK SWITCH
360
YES
GFX_TYPE = 1111 ?
NO
362
GFX_HEADER 2
364
GFX_CONTENT
366
WORD IS DATA ?
YES
NO
368
PIPE_COMP

FIG. 9

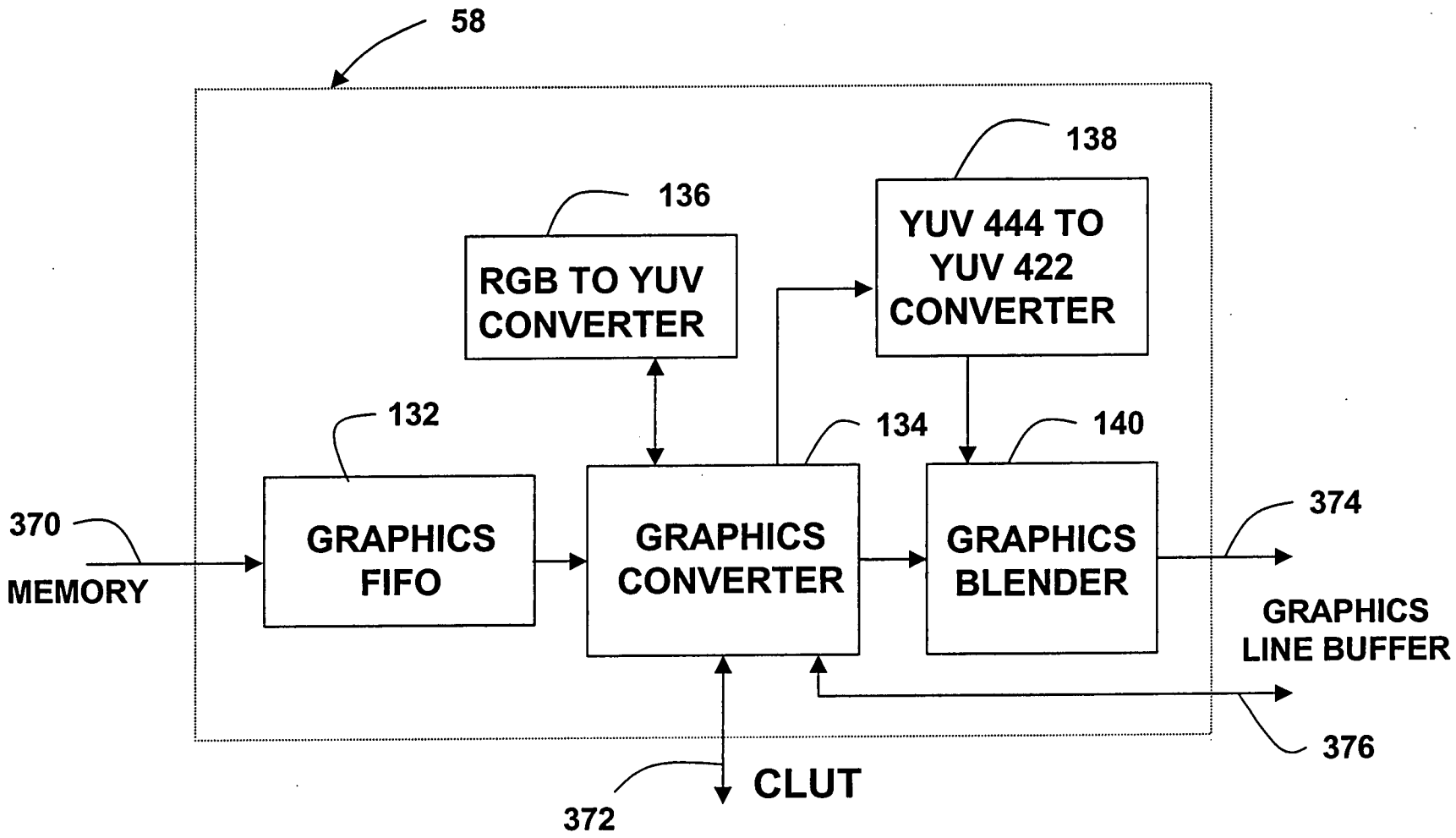
58
138
136
YUV 444 TO
YUV 422
CONVERTER
RGB TO YUV
CONVERTER
132
134
140
370
MEMORY
GRAPHICS
FIFO
GRAPHICS
CONVERTER
GRAPHICS
BLENDER
374
GRAPHICS
LINE BUFFER
376
CLUT
372

FIG. 10

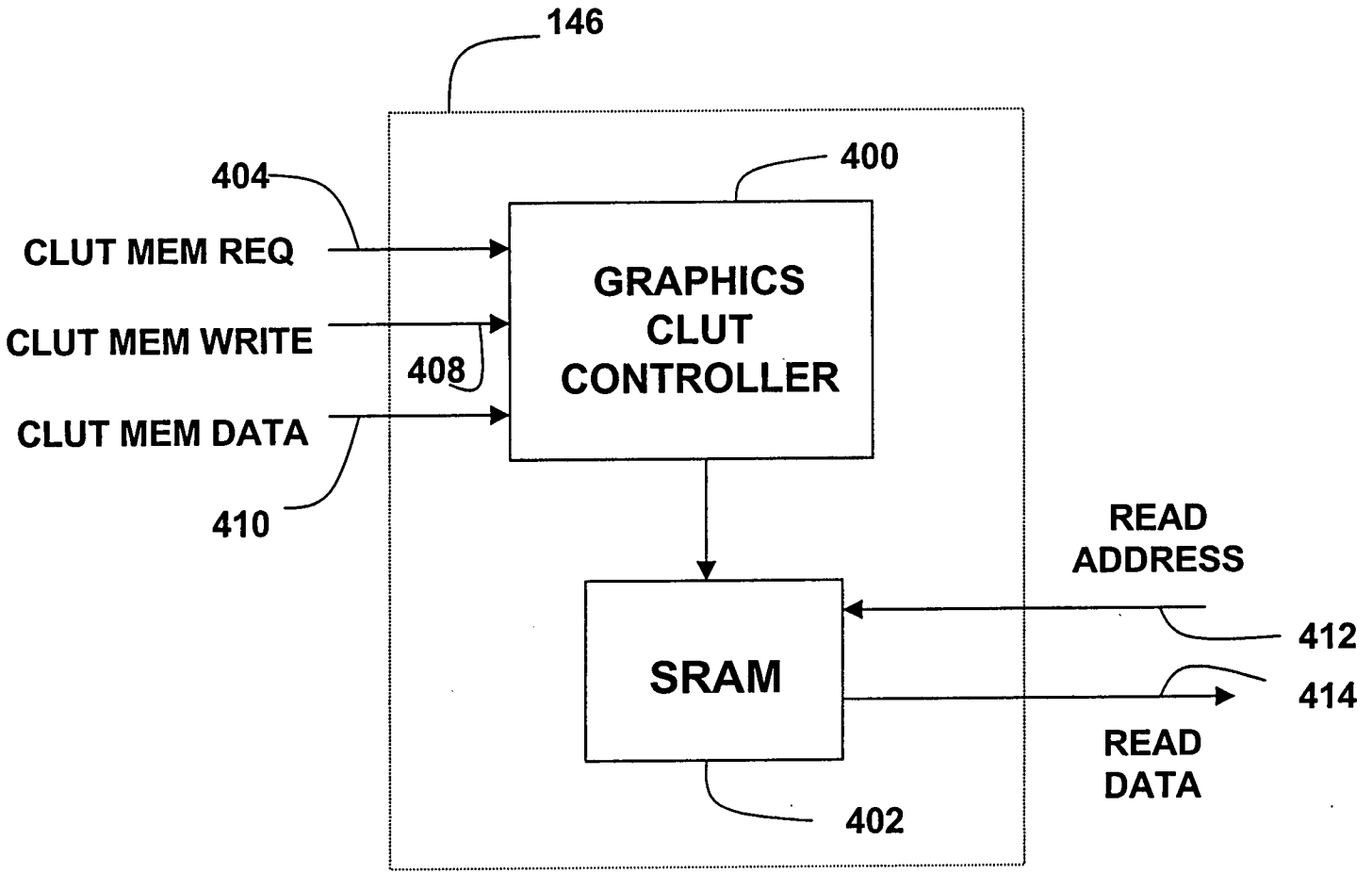

FIG. 11

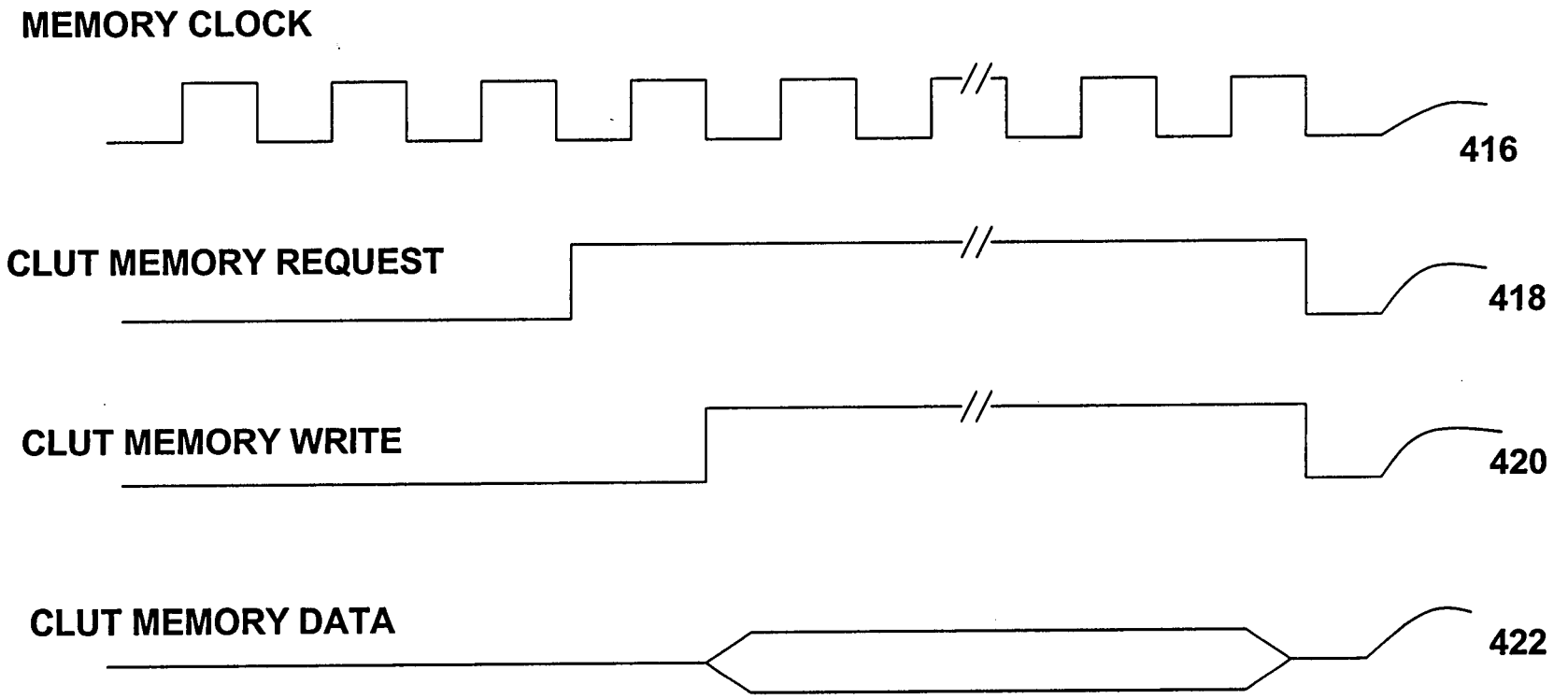

FIG. 12

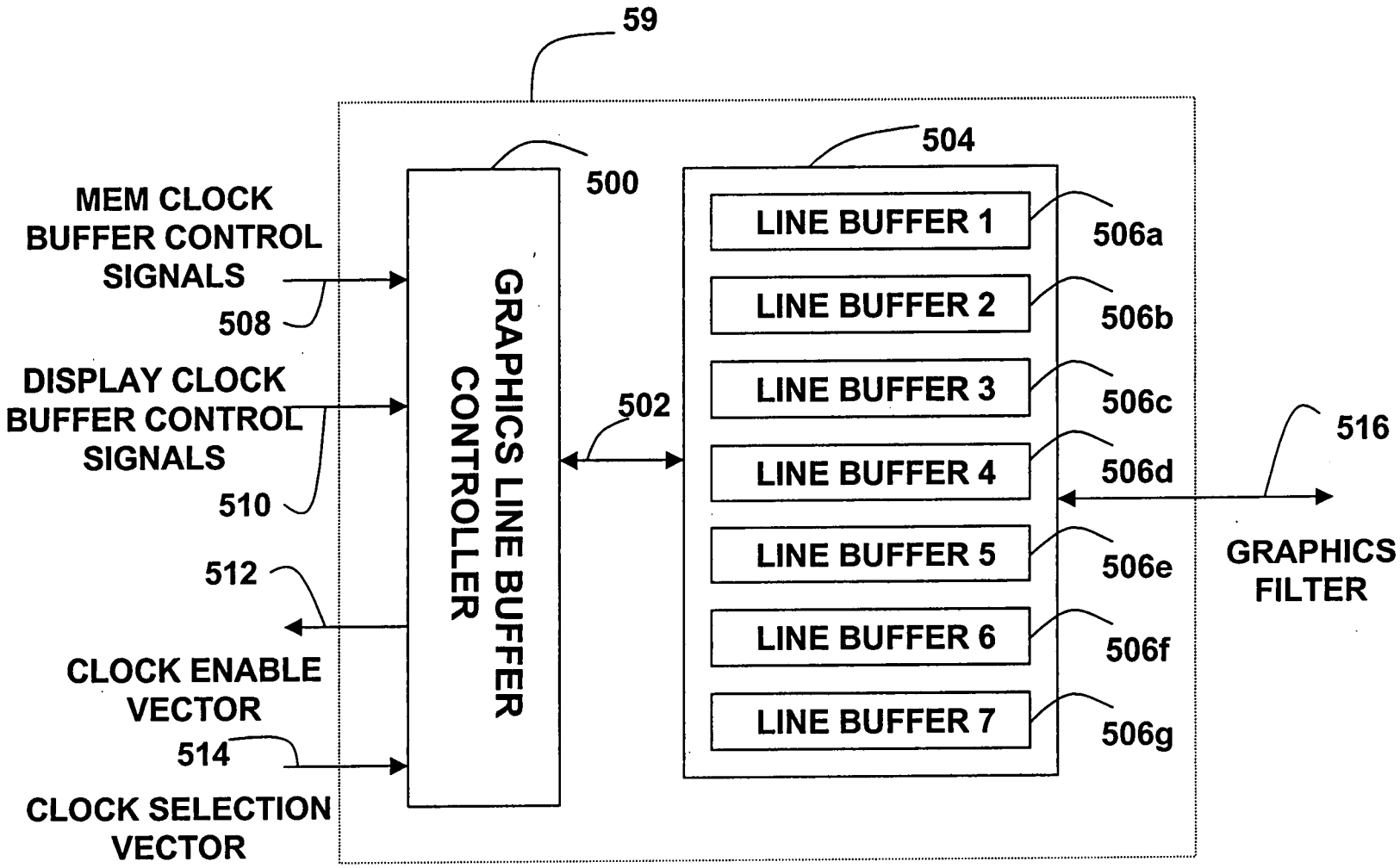
59
500
504
MEM CLOCK BUFFER CONTROL SIGNALS
508
DISPLAY CLOCK BUFFER CONTROL SIGNALS
510
512
CLOCK ENABLE VECTOR
514
CLOCK SELECTION VECTOR
GRAPHICS LINE BUFFER CONTROLLER
502
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
LINE BUFFER 6
LINE BUFFER 7
506a
506b
506c
506d
506e
506f
506g
516
GRAPHICS FILTER

FIG. 13

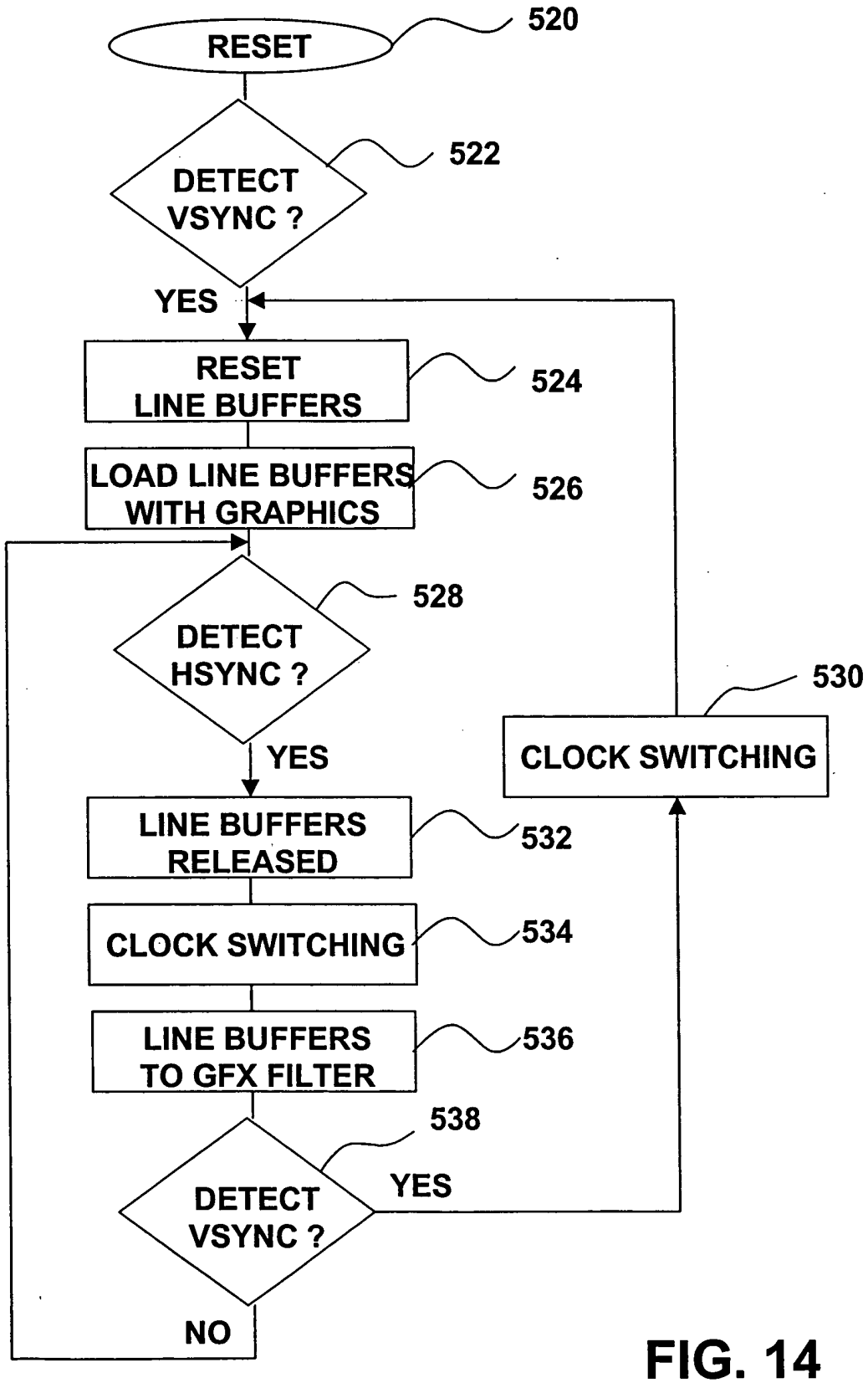
RESET
520
DETECT VSYNC ?
522
YES
RESET LINE BUFFERS
524
LOAD LINE BUFFERS WITH GRAPHICS
526
DETECT HSYNC ?
528
YES
LINE BUFFERS RELEASED
532
CLOCK SWITCHING
534
LINE BUFFERS TO GFX FILTER
536
DETECT VSYNC ?
538
YES
NO
CLOCK SWITCHING
530

FIG. 14

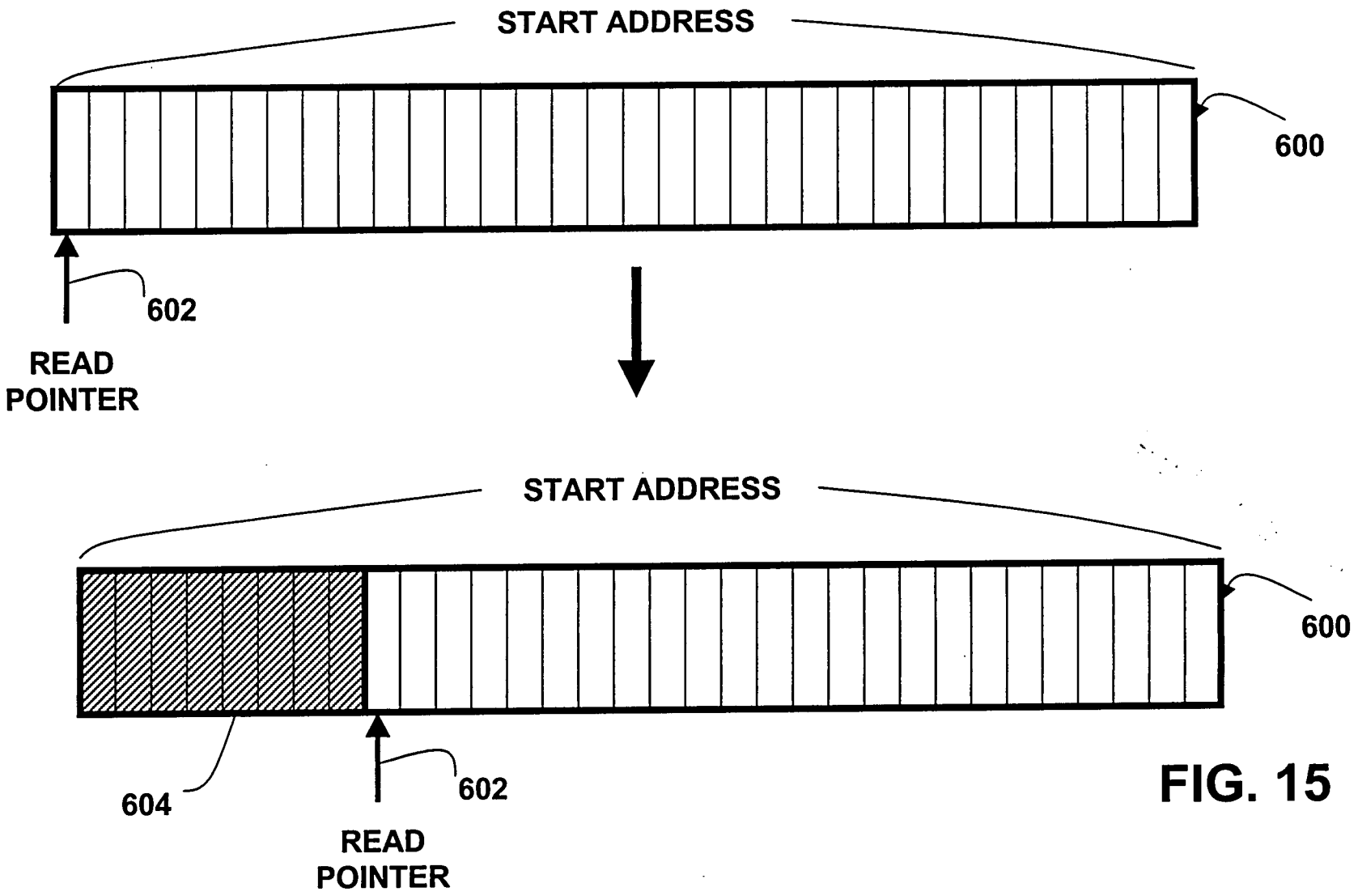

FIG. 15

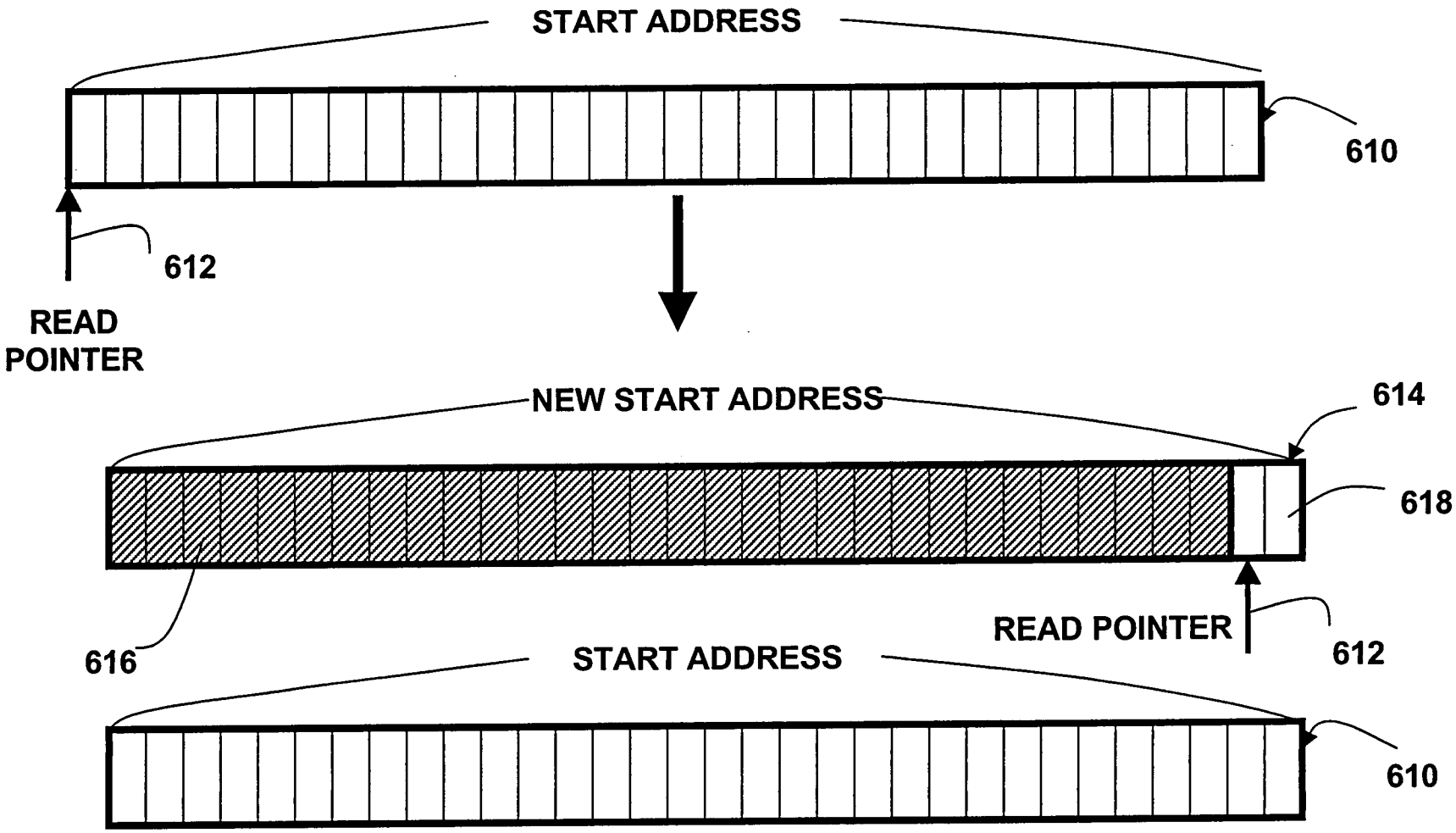

FIG. 16

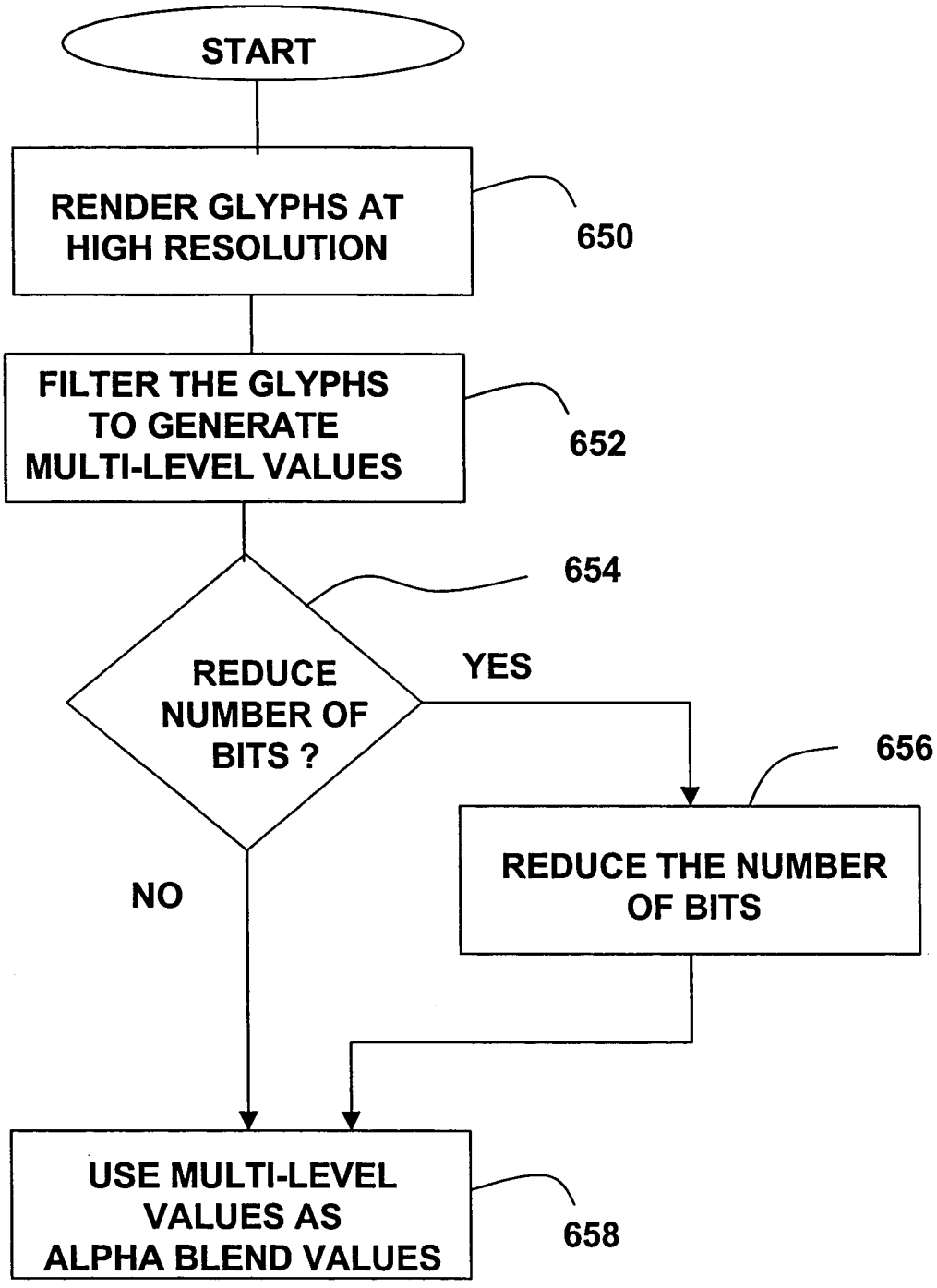
START
RENDER GLYPHS AT HIGH RESOLUTION
650
FILTER THE GLYPHS TO GENERATE MULTI-LEVEL VALUES
652
654
REDUCE NUMBER OF BITS ?
YES
NO
656
REDUCE THE NUMBER OF BITS
USE MULTI-LEVEL VALUES AS ALPHA BLEND VALUES
658

FIG. 17

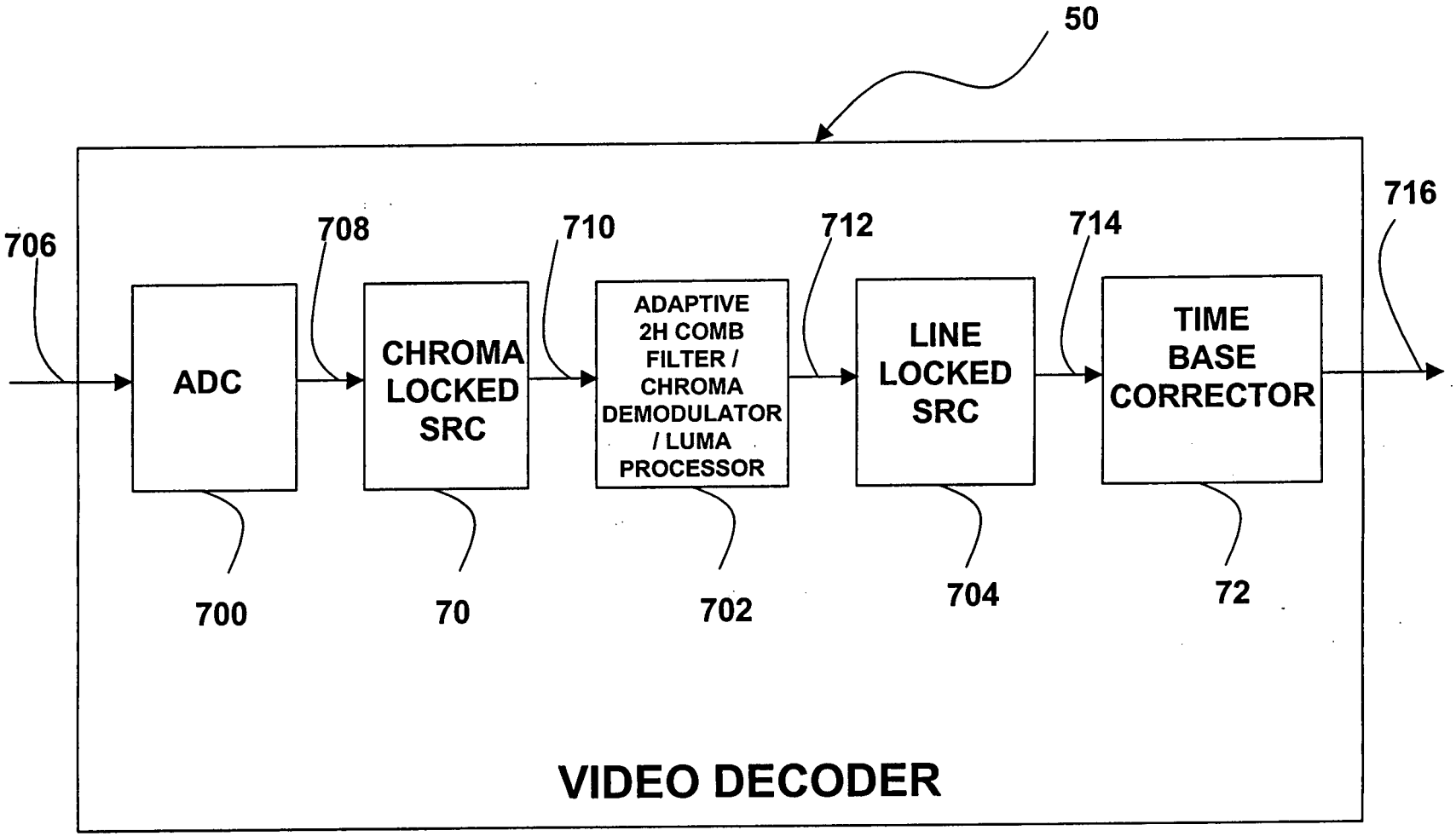

FIG. 18

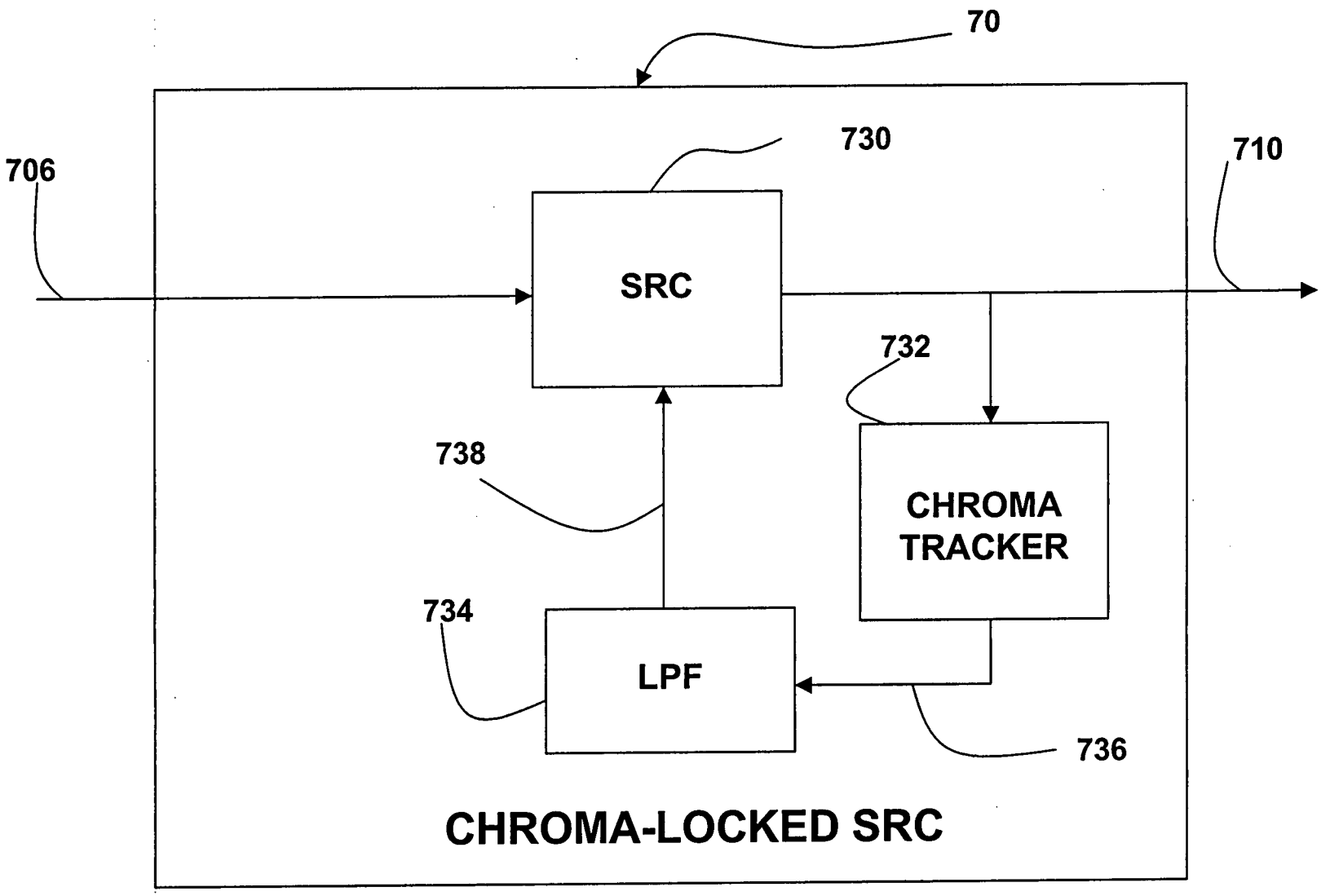

FIG. 19

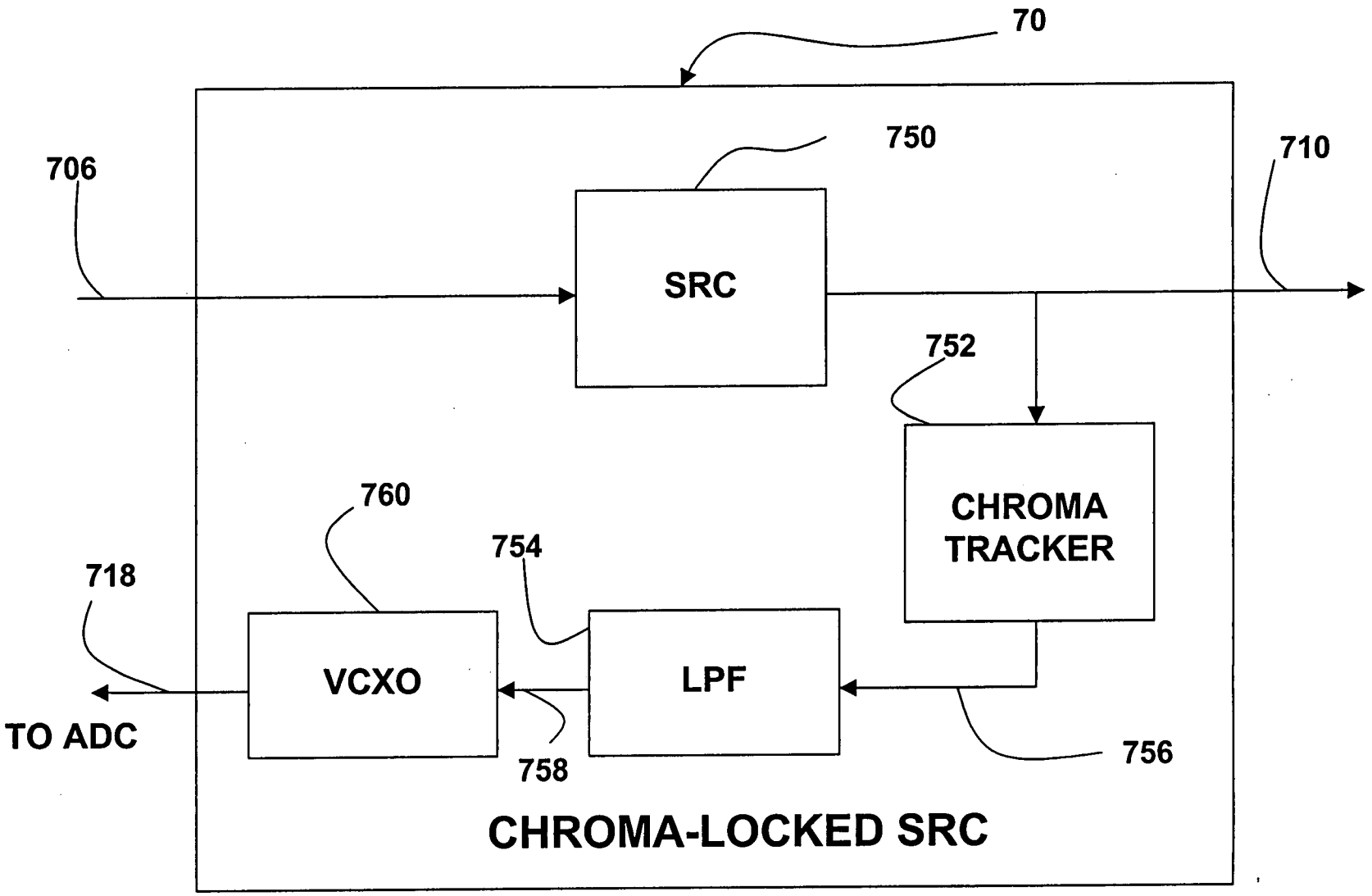

FIG. 20

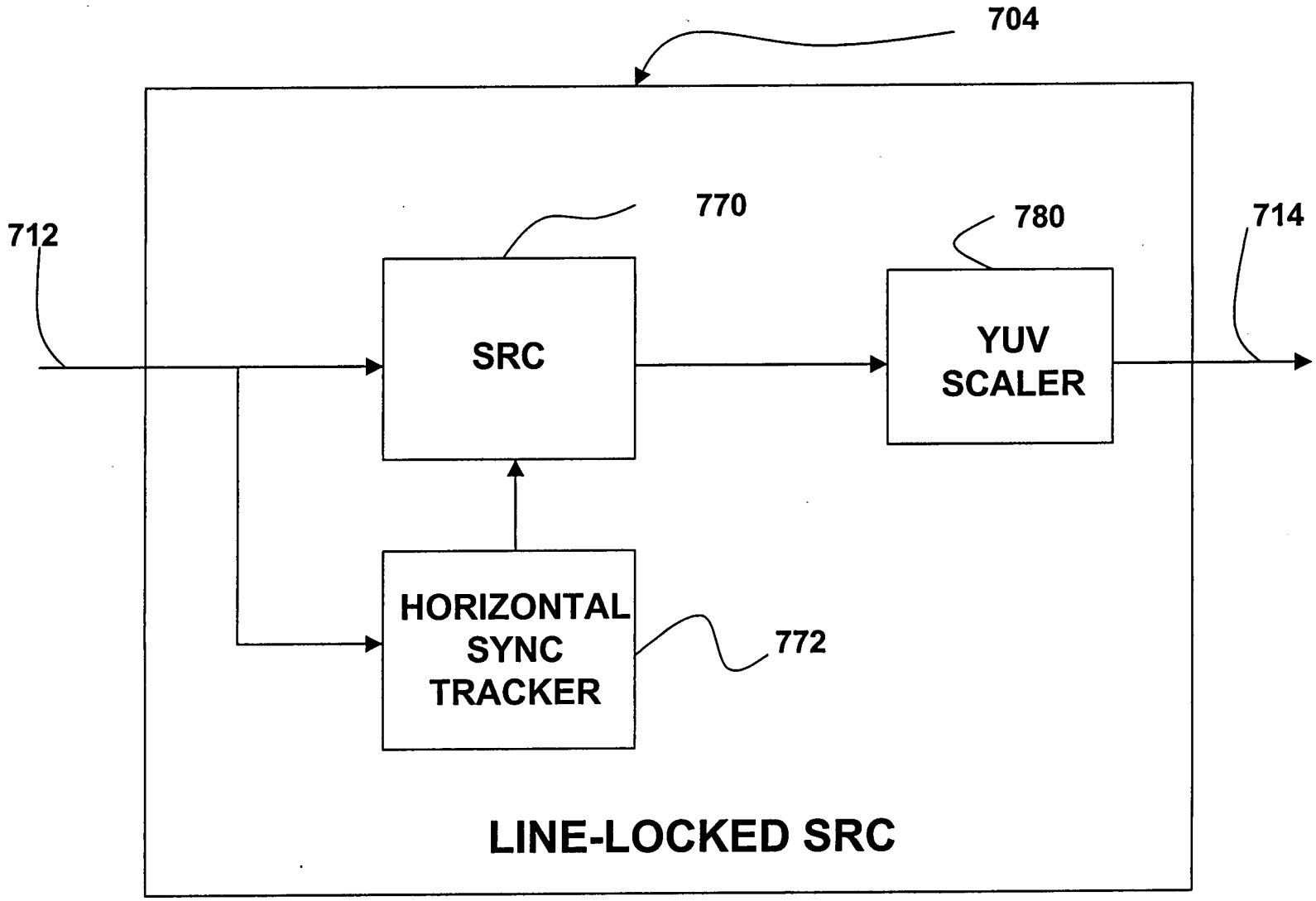

FIG. 21

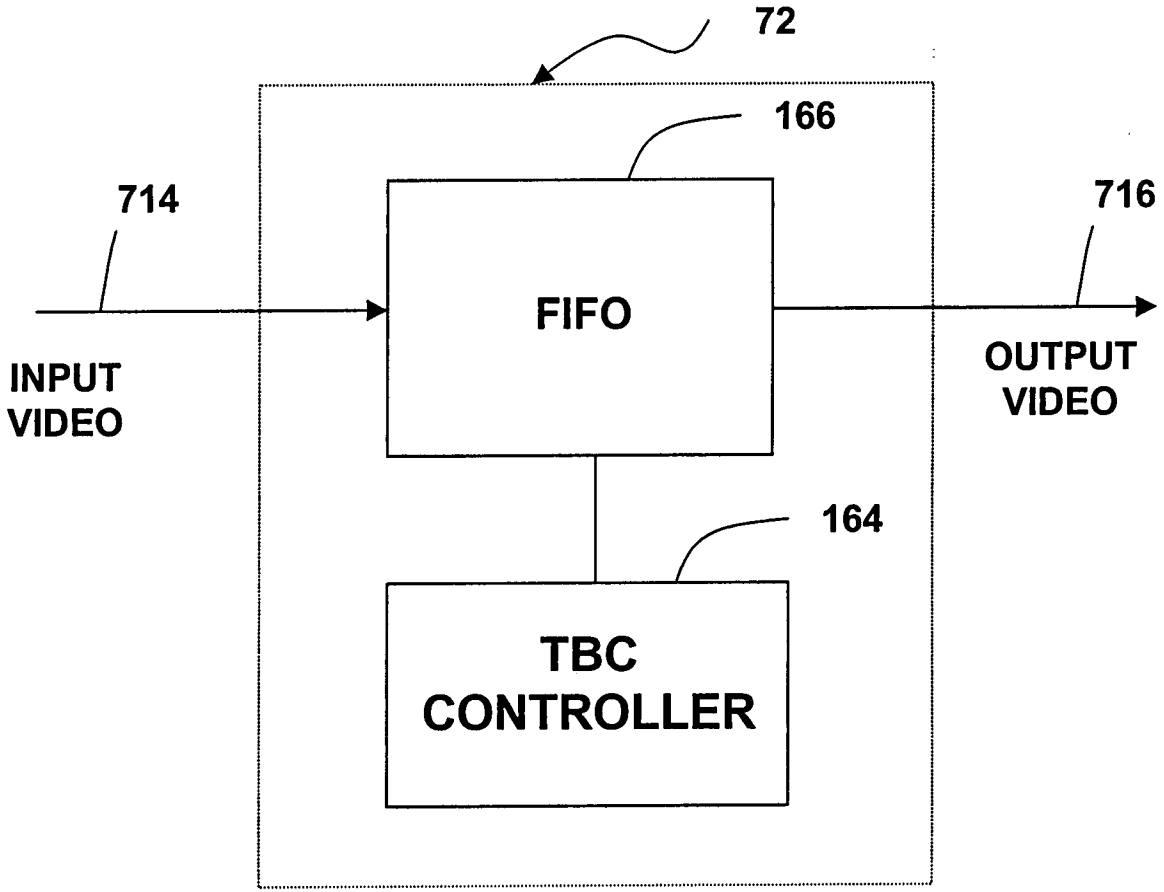
72
166
714
716
FIFO
INPUT
VIDEO
OUTPUT
VIDEO
164
TBC
CONTROLLER

FIG. 22

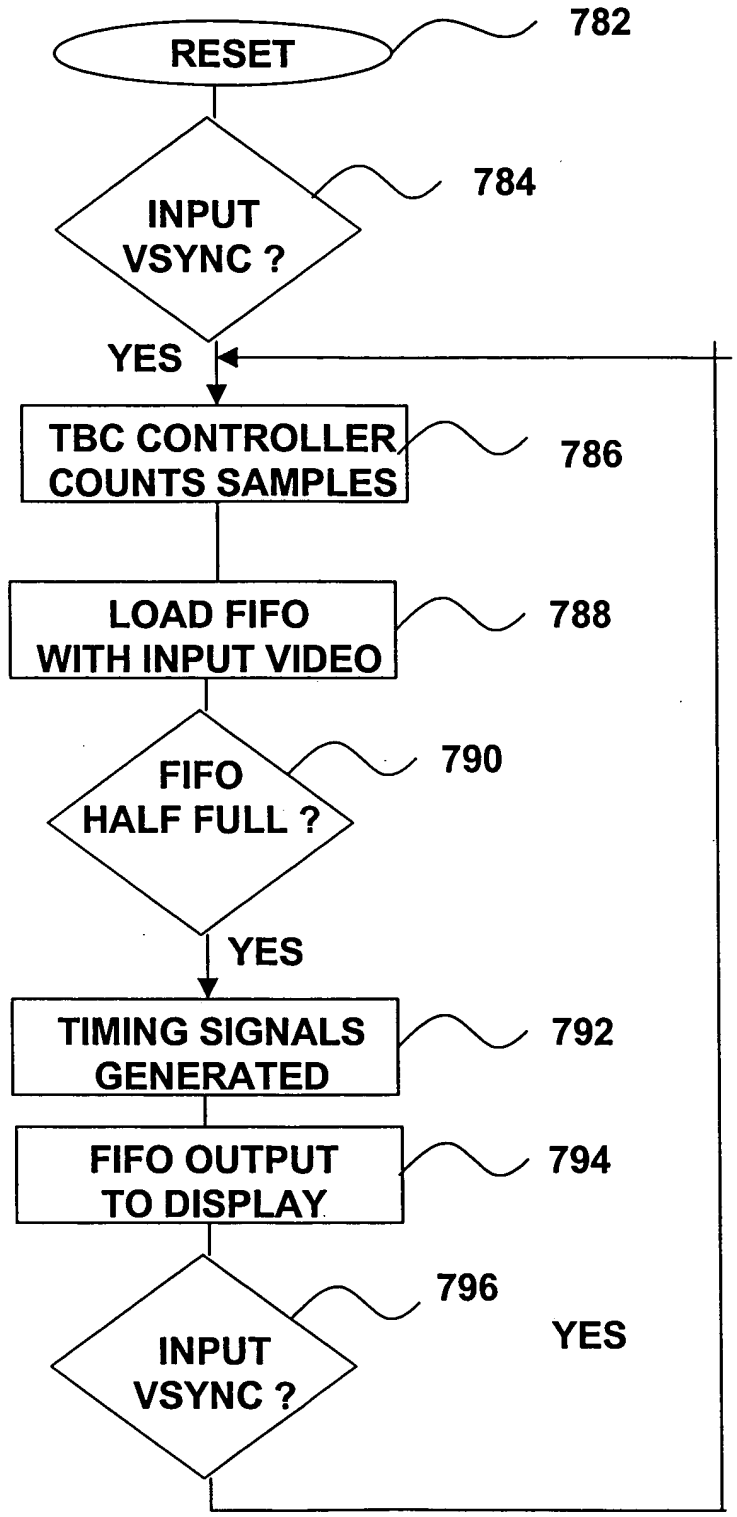
RESET
782
INPUT VSYNC ?
784
YES
TBC CONTROLLER COUNTS SAMPLES
786
LOAD FIFO WITH INPUT VIDEO
788
FIFO HALF FULL ?
790
YES
TIMING SIGNALS GENERATED
792
FIFO OUTPUT TO DISPLAY
794
INPUT VSYNC ?
796
YES

FIG. 23

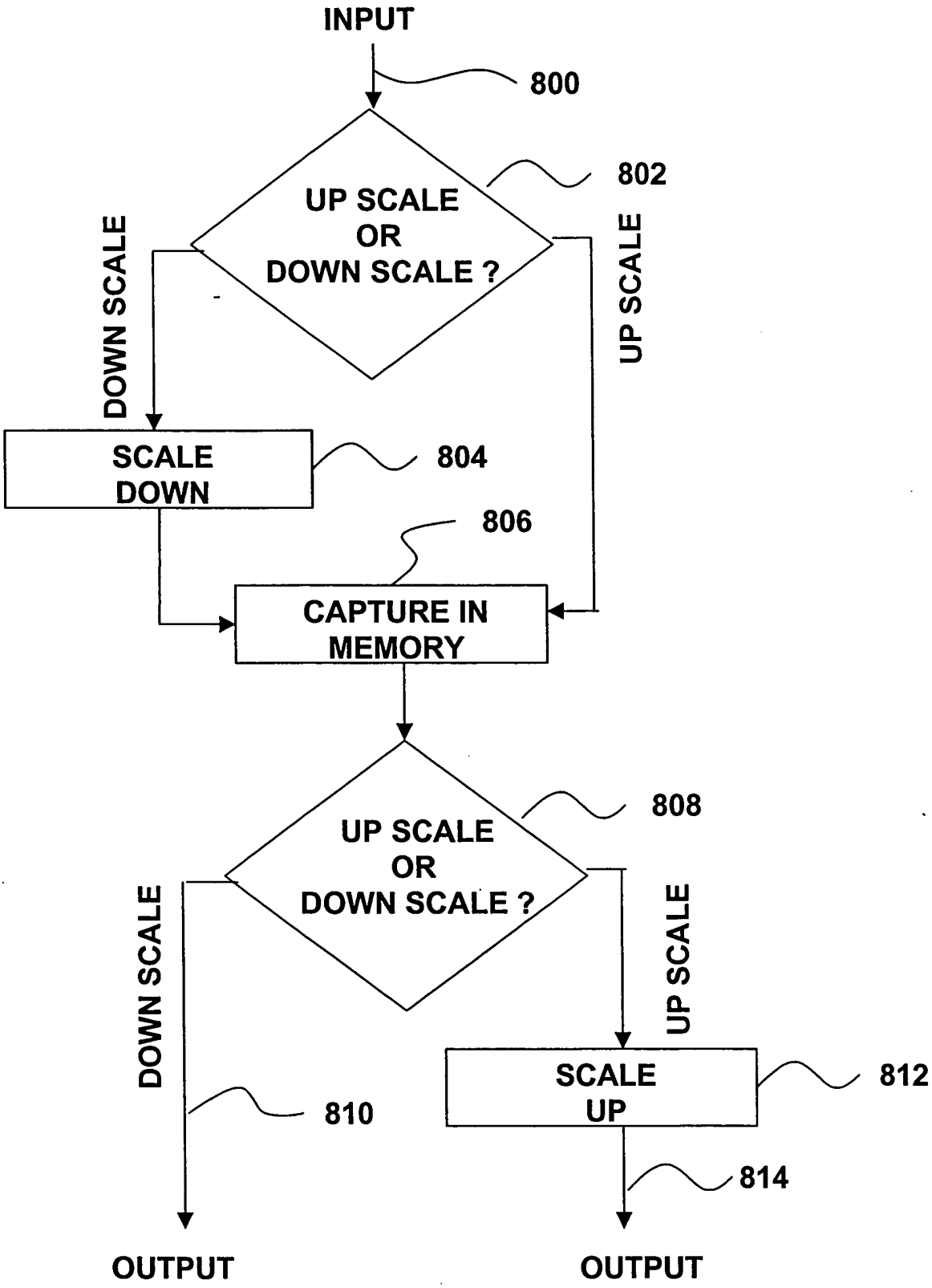
INPUT
800
UP SCALE OR DOWN SCALE ?
802
DOWN SCALE
UP SCALE
SCALE DOWN
804
806
CAPTURE IN MEMORY
UP SCALE OR DOWN SCALE ?
808
DOWN SCALE
UP SCALE
SCALE UP
812
810
814
OUTPUT
OUTPUT

FIG. 24

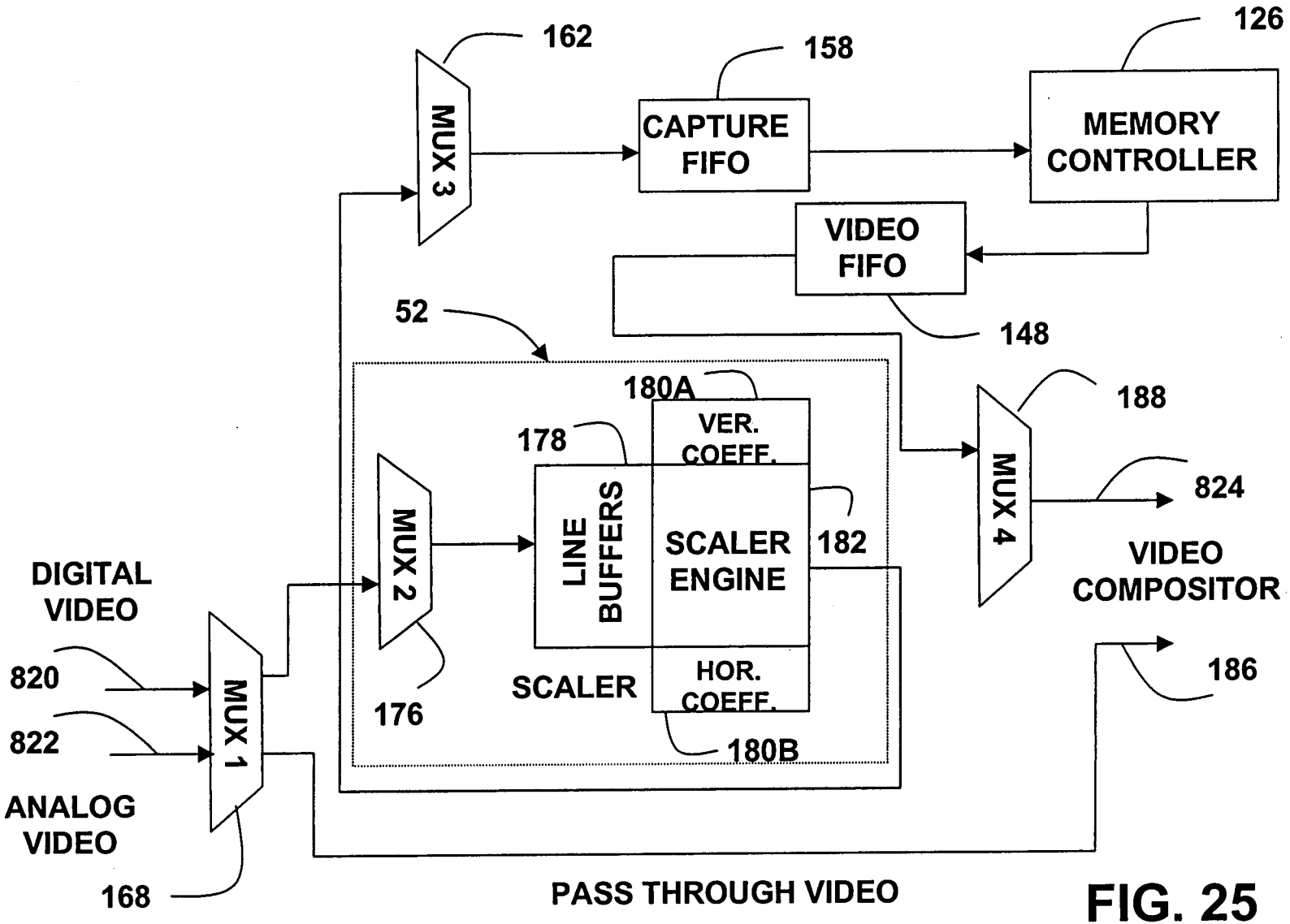
162
158
126
MUX 3
CAPTURE FIFO
MEMORY CONTROLLER
VIDEO FIFO
148
52
180A
188
178
VER. COEFF.
MUX 4
824
MUX 2
LINE BUFFERS
SCALER ENGINE
182
VIDEO COMPOSITOR
DIGITAL VIDEO
820
SCALER
HOR. COEFF.
186
MUX 1
822
176
180B
ANALOG VIDEO
168
PASS THROUGH VIDEO

FIG. 25

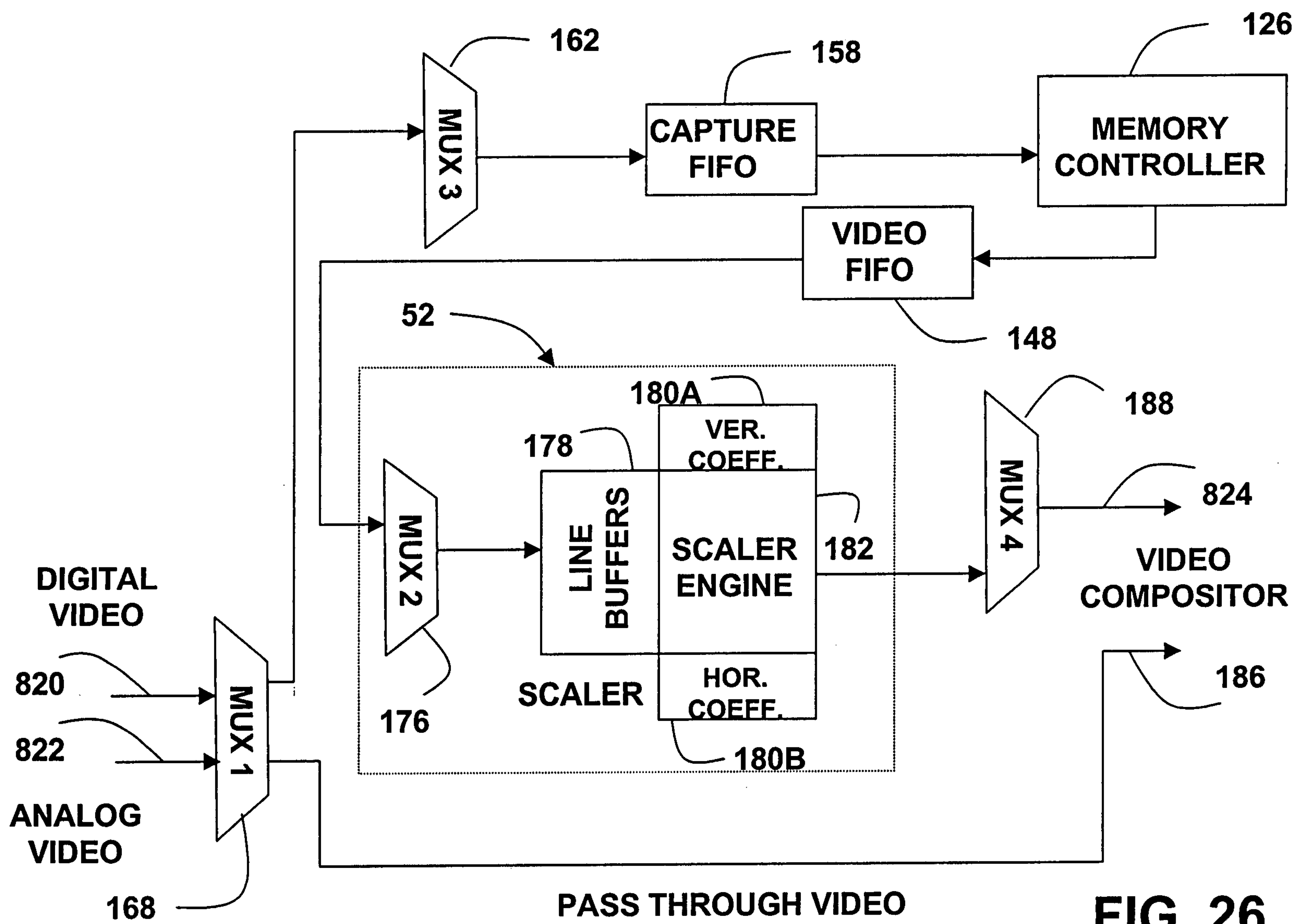

FIG. 26

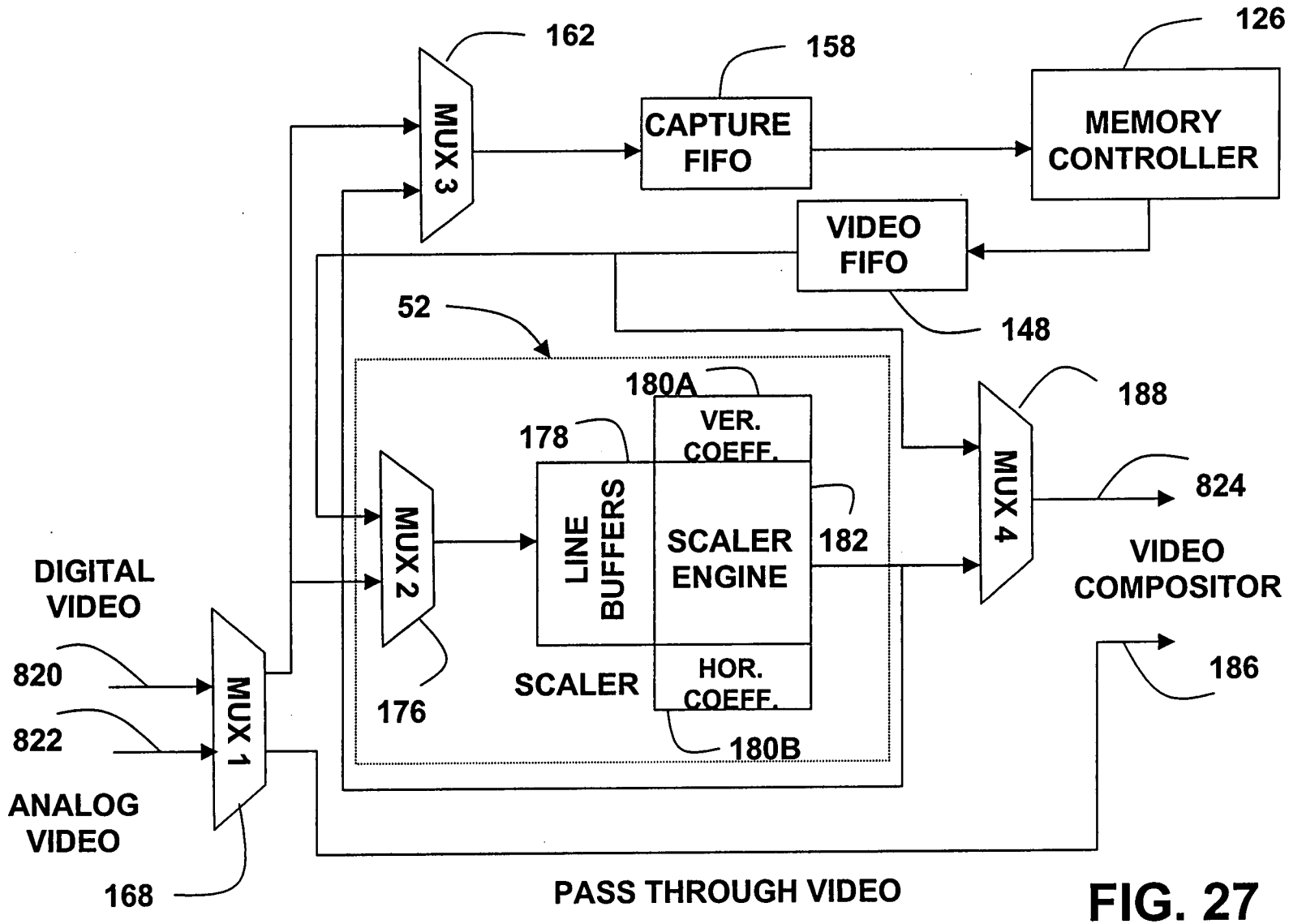

FIG. 27

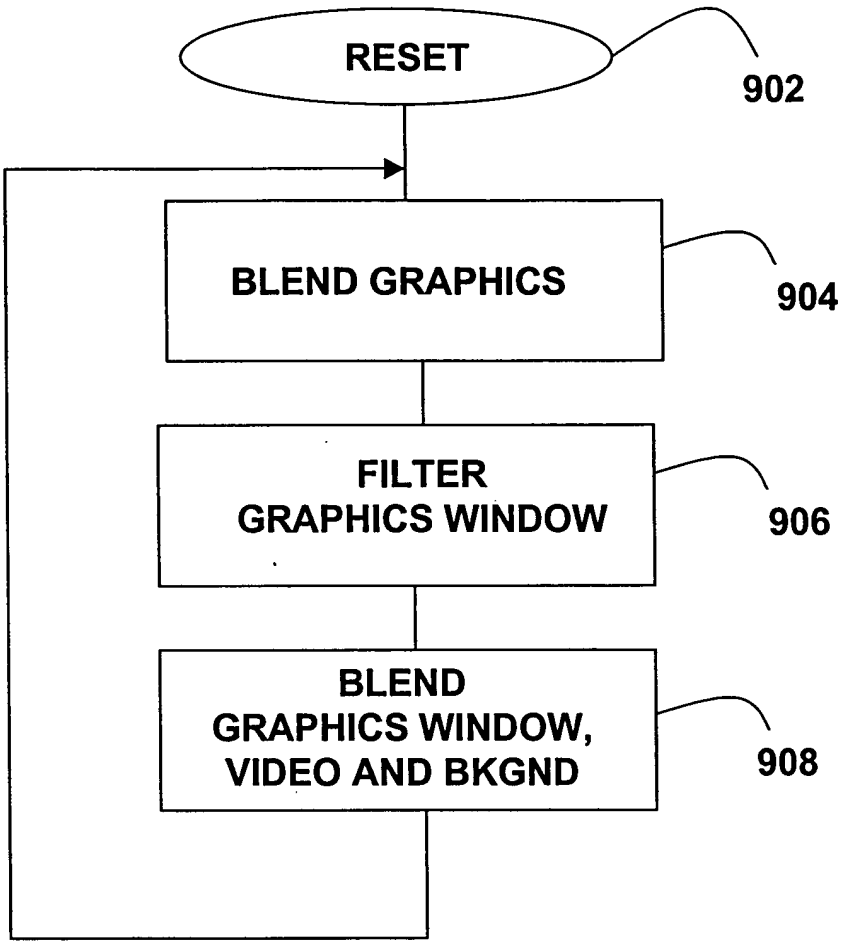
RESET
902
BLEND GRAPHICS
904
FILTER
GRAPHICS WINDOW
906
BLEND
GRAPHICS WINDOW,
VIDEO AND BKGND
908

FIG. 28

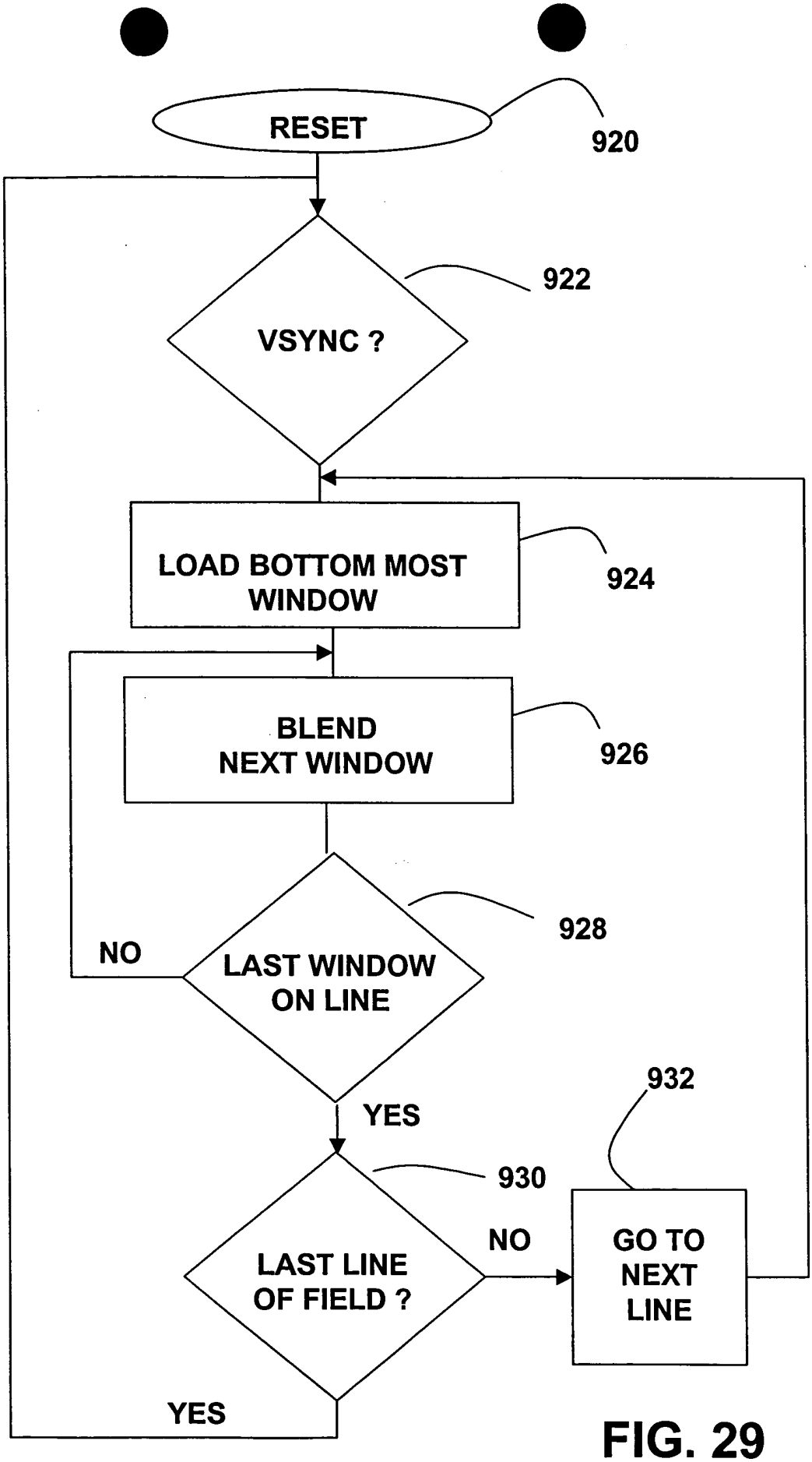
RESET
920
VSYNC ?
922
LOAD BOTTOM MOST WINDOW
924
BLEND NEXT WINDOW
926
LAST WINDOW ON LINE
928
NO
YES
LAST LINE OF FIELD ?
930
NO
GO TO NEXT LINE
932
YES

FIG. 29

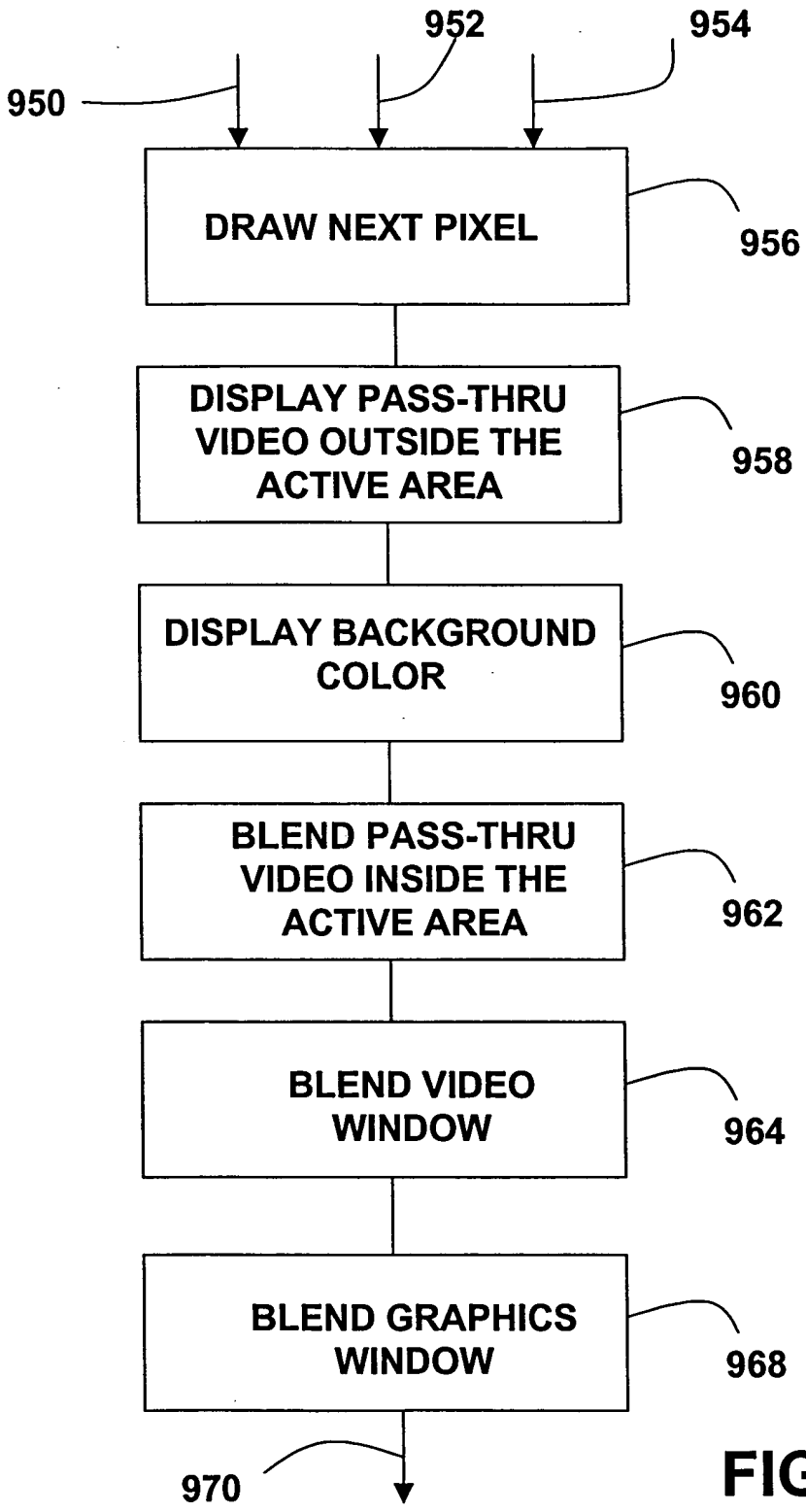
950
952
954
DRAW NEXT PIXEL
956
DISPLAY PASS-THRU VIDEO OUTSIDE THE ACTIVE AREA
958
DISPLAY BACKGROUND COLOR
960
BLEND PASS-THRU VIDEO INSIDE THE ACTIVE AREA
962
BLEND VIDEO WINDOW
964
BLEND GRAPHICS WINDOW
968
970

FIG. 30

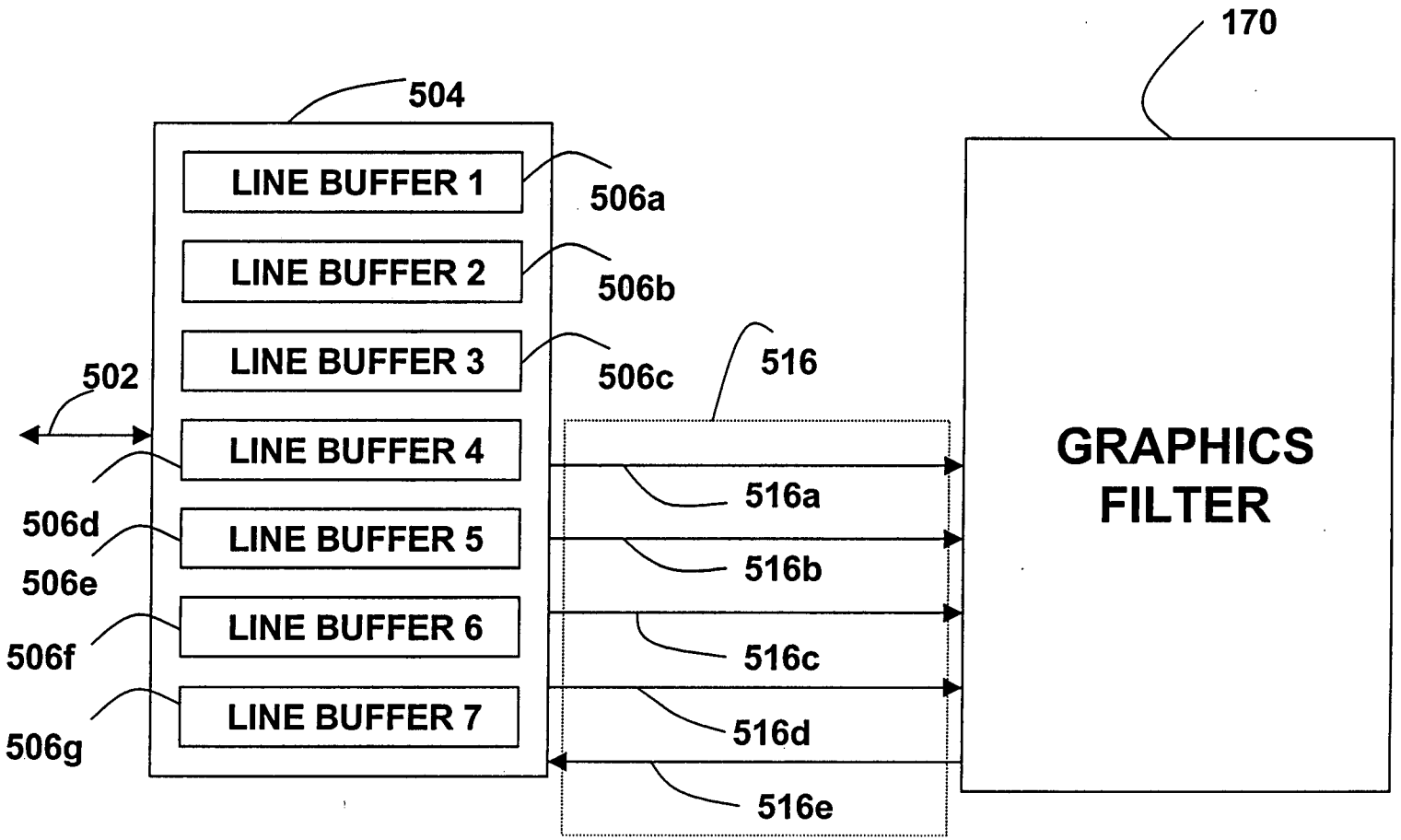
170
504
LINE BUFFER 1
506a
LINE BUFFER 2
506b
LINE BUFFER 3
506c
516
502
LINE BUFFER 4
516a
506d
LINE BUFFER 5
516b
506e
LINE BUFFER 6
506f
516c
LINE BUFFER 7
516d
506g
516e
GRAPHICS FILTER

FIG. 31

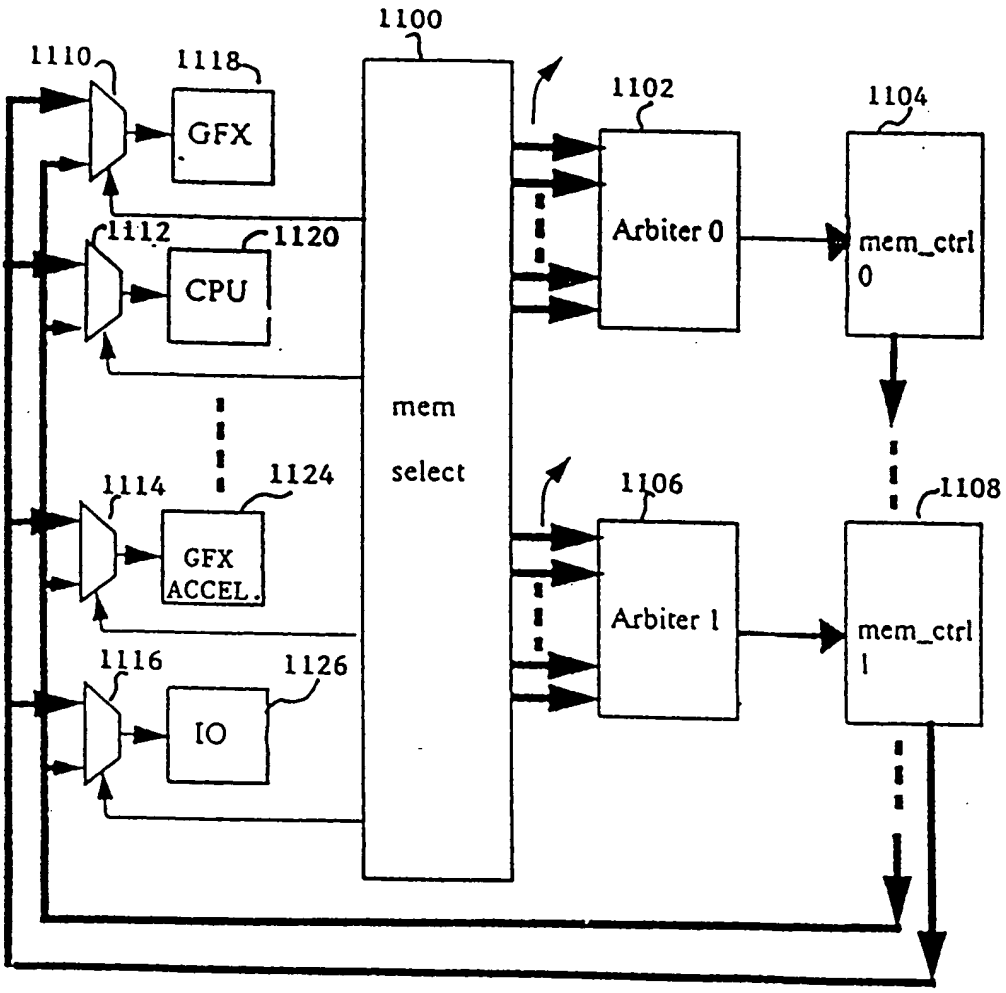
1100
1110
1118
GFX
1102
1104
Arbiter 0
mem_ctrl 0
1112
1120
CPU
mem
select
1114
1124
GFX ACCEL.
1106
1108
Arbiter 1
mem_ctrl 1
1116
1126
IO

FIG. 32

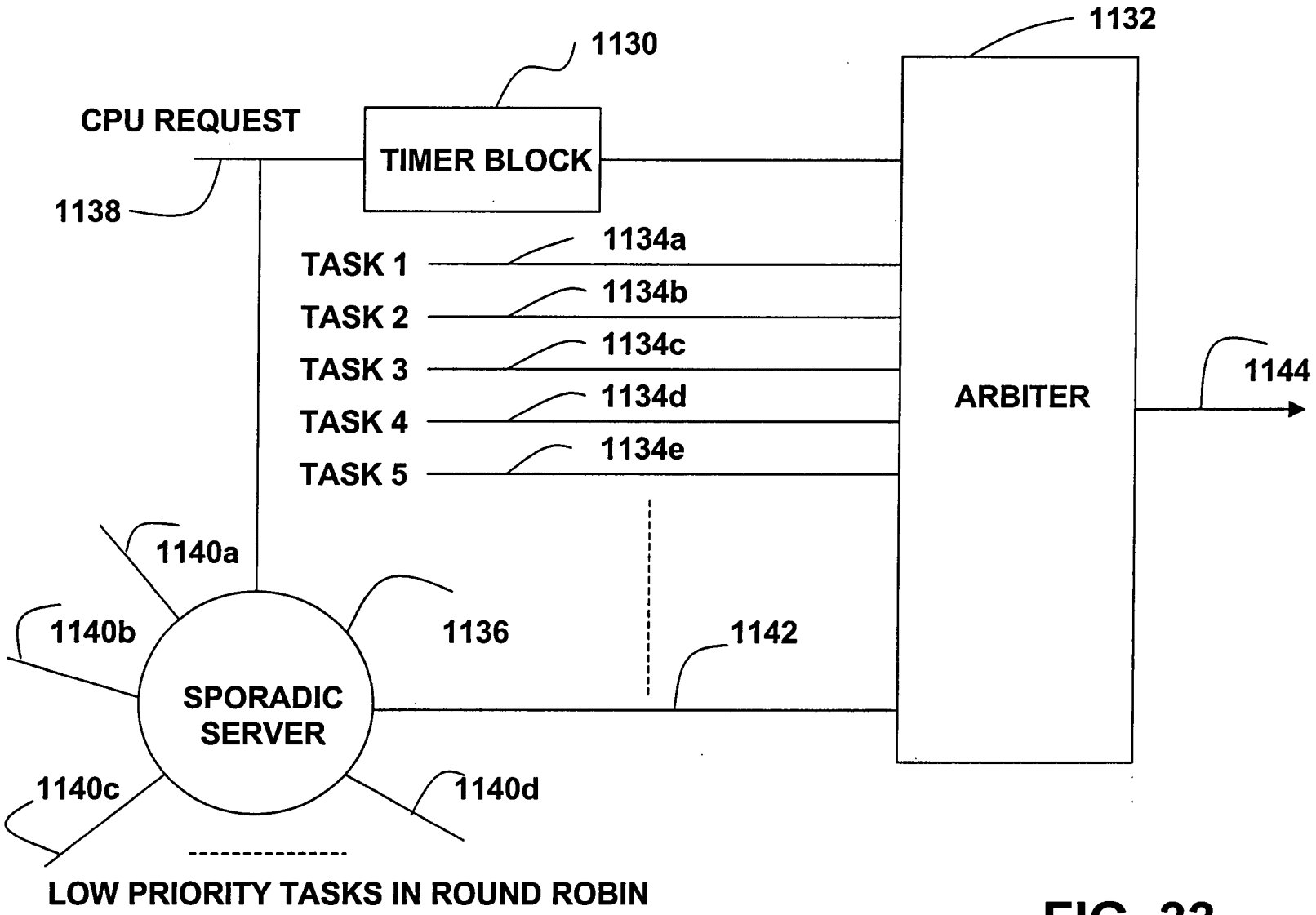

FIG. 33

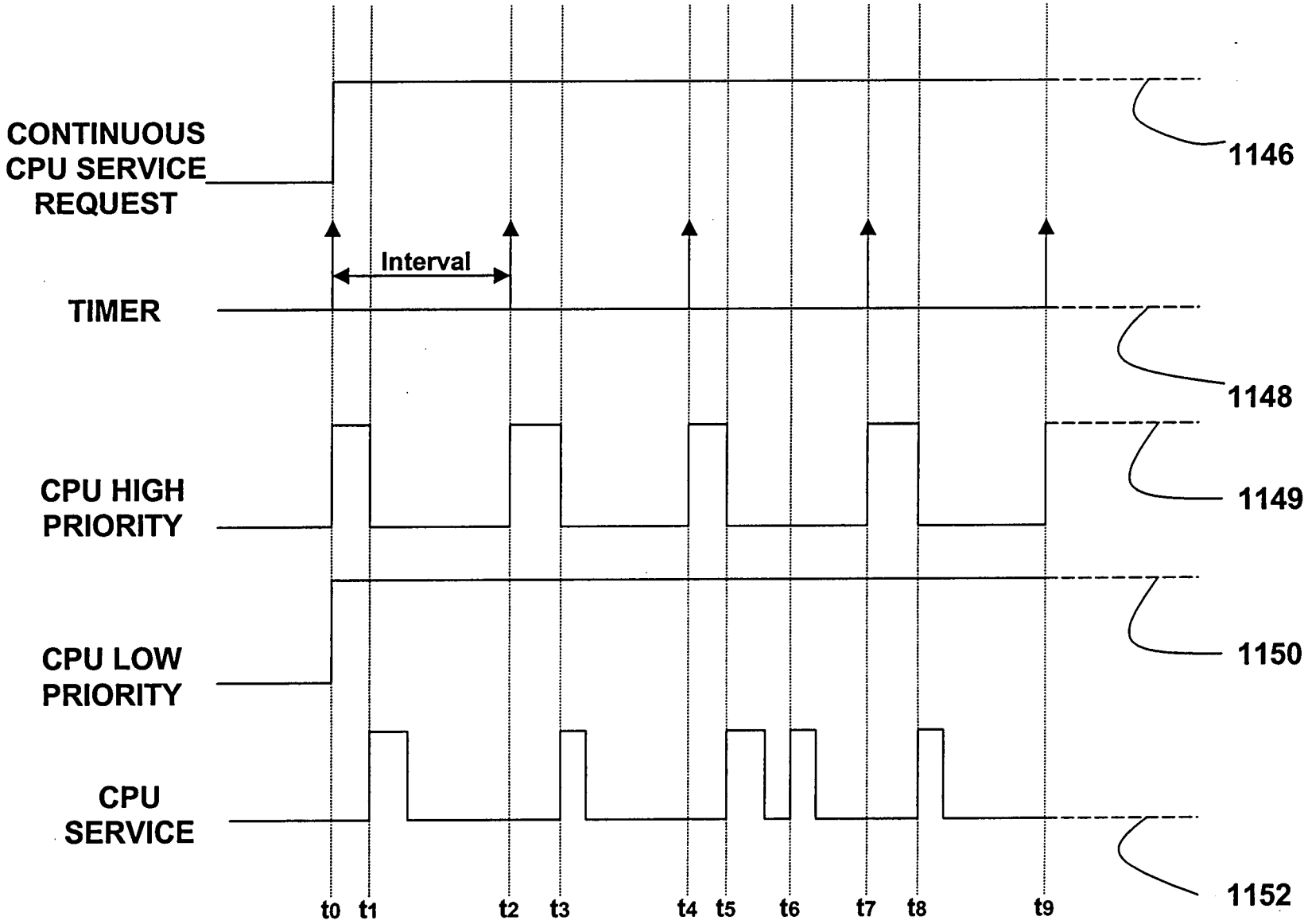
CONTINUOUS CPU SERVICE REQUEST
Interval
TIMER
CPU HIGH PRIORITY
CPU LOW PRIORITY
CPU SERVICE
1146
1148
1149
1150
1152
t0
t1
t2
t3
t4
t5
t6
t7
t8
t9

FIG. 34

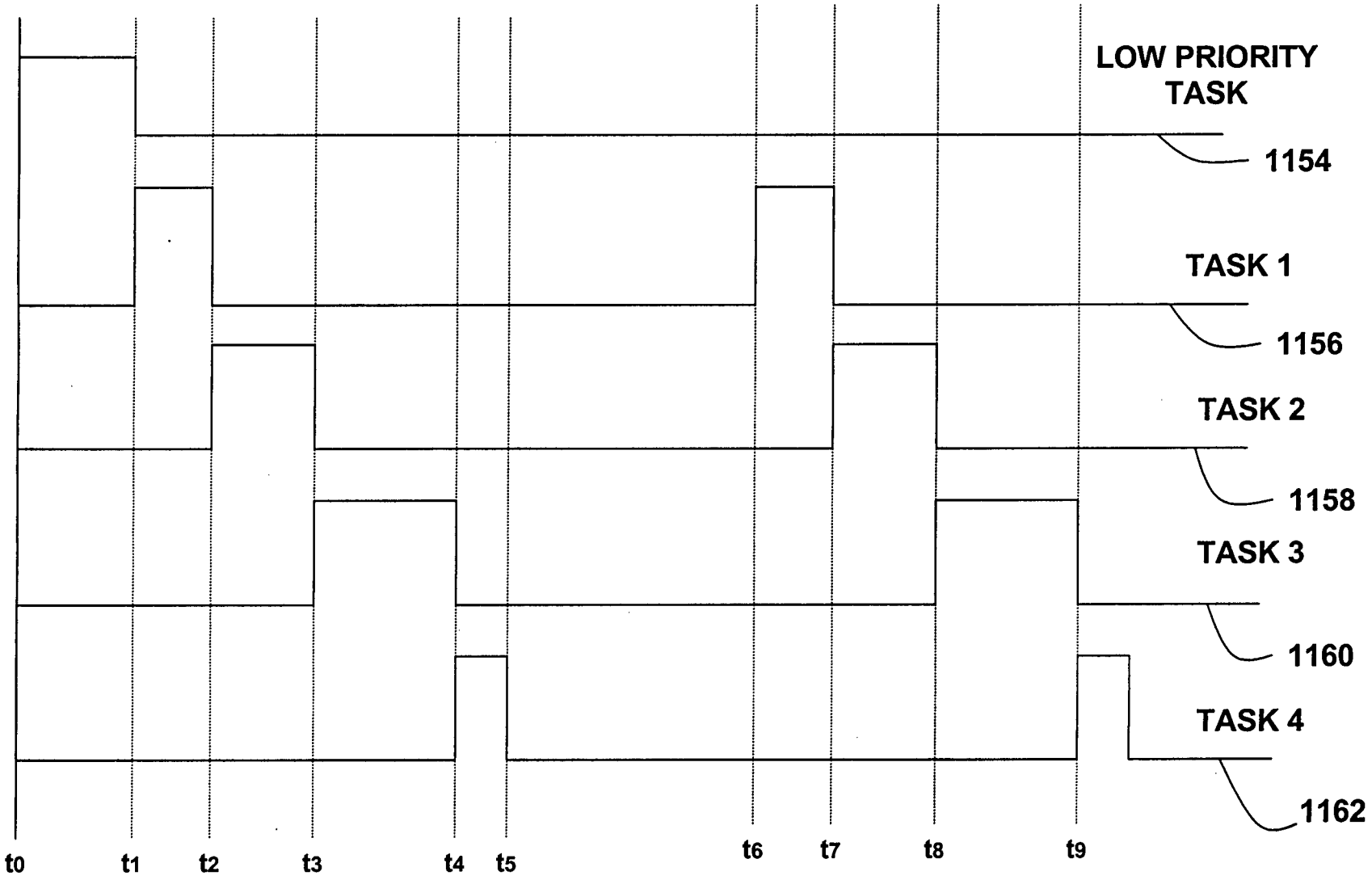

FIG. 35

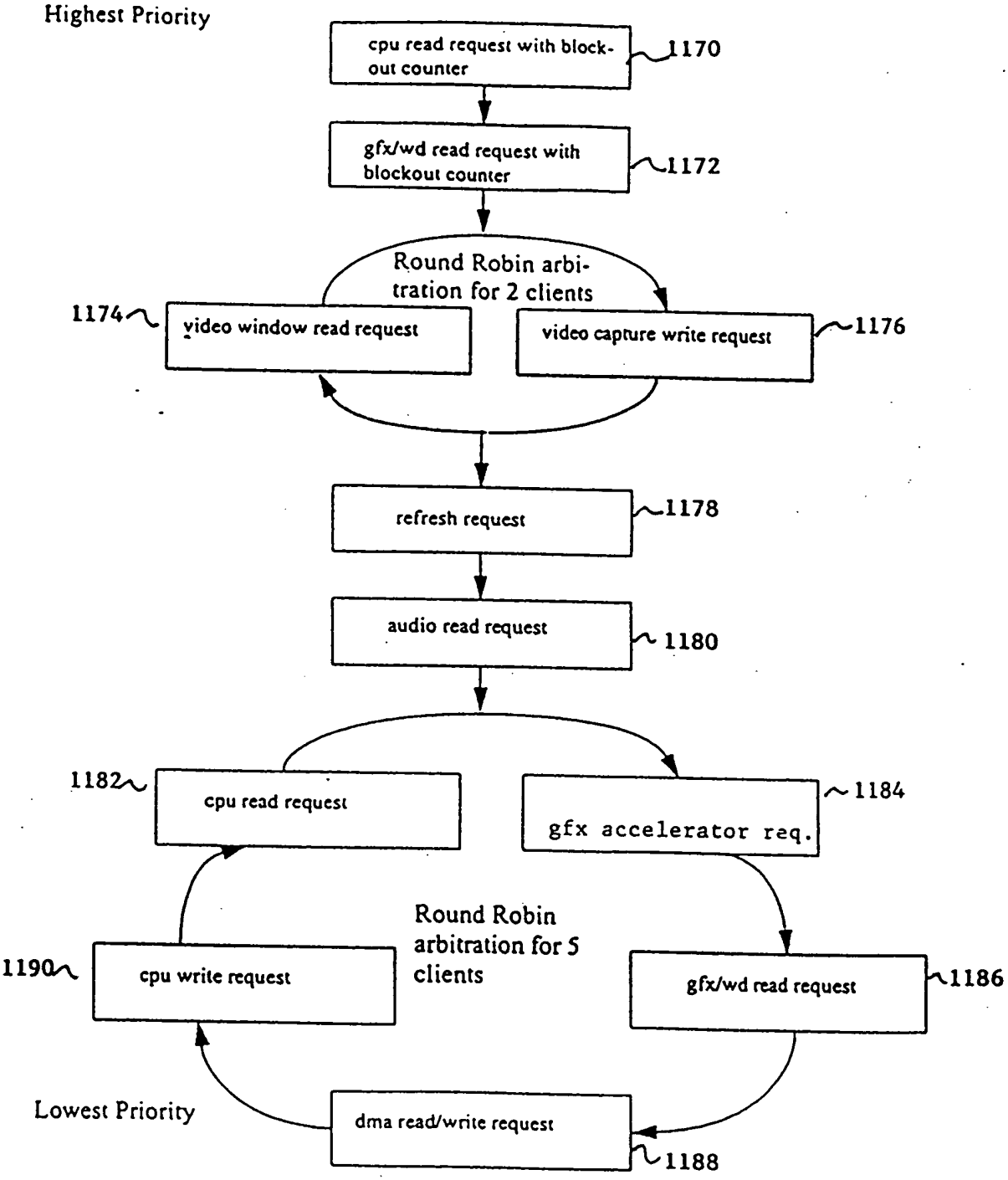
Highest Priority
cpu read request with block-out counter
1170
gfx/wd read request with blockout counter
1172
Round Robin arbitration for 2 clients
1174
video window read request
video capture write request
1176
refresh request
1178
audio read request
1180
1182
cpu read request
gfx accelerator req.
1184
Round Robin arbitration for 5 clients
1190
cpu write request
gfx/wd read request
1186
Lowest Priority
dma read/write request
1188

FIG. 36

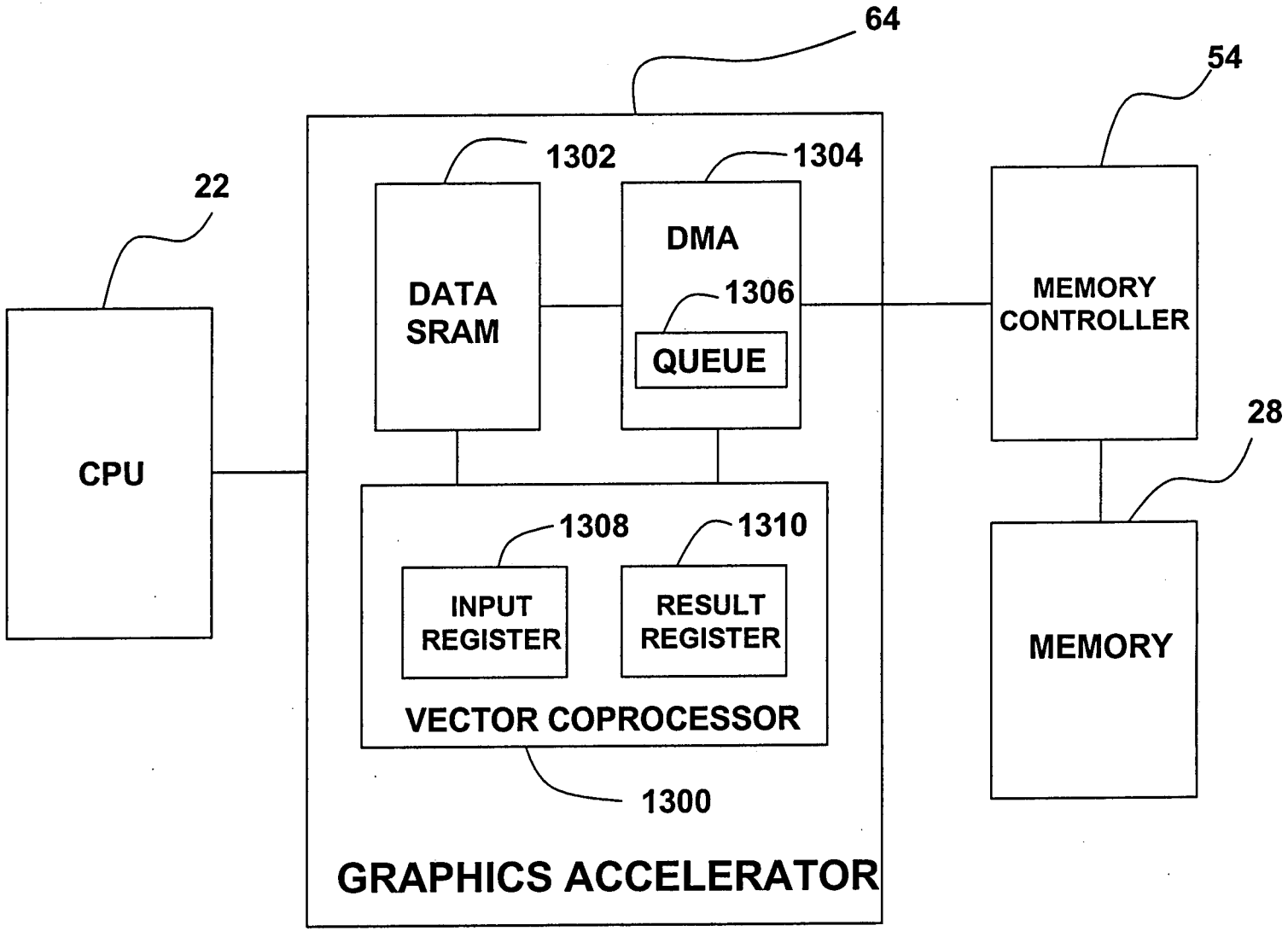

FIG. 37

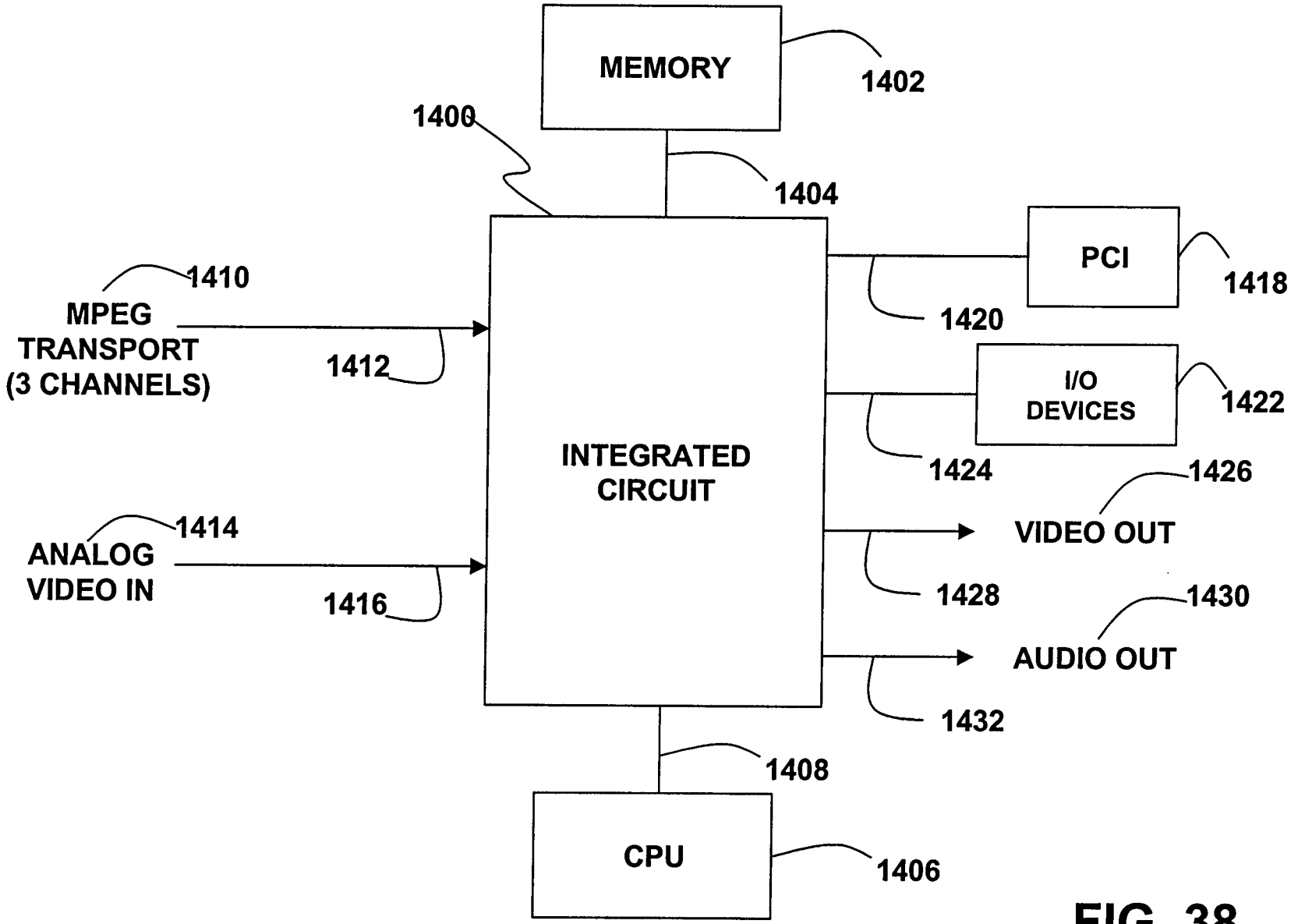
MEMORY
1402
1400
1404
PCI
1418
1410
MPEG
TRANSPORT
(3 CHANNELS)
1412
1420
I/O
DEVICES
1422
INTEGRATED
CIRCUIT
1424
1426
VIDEO OUT
1414
ANALOG
VIDEO IN
1416
1428
1430
AUDIO OUT
1432
1408
CPU
1406

FIG. 38

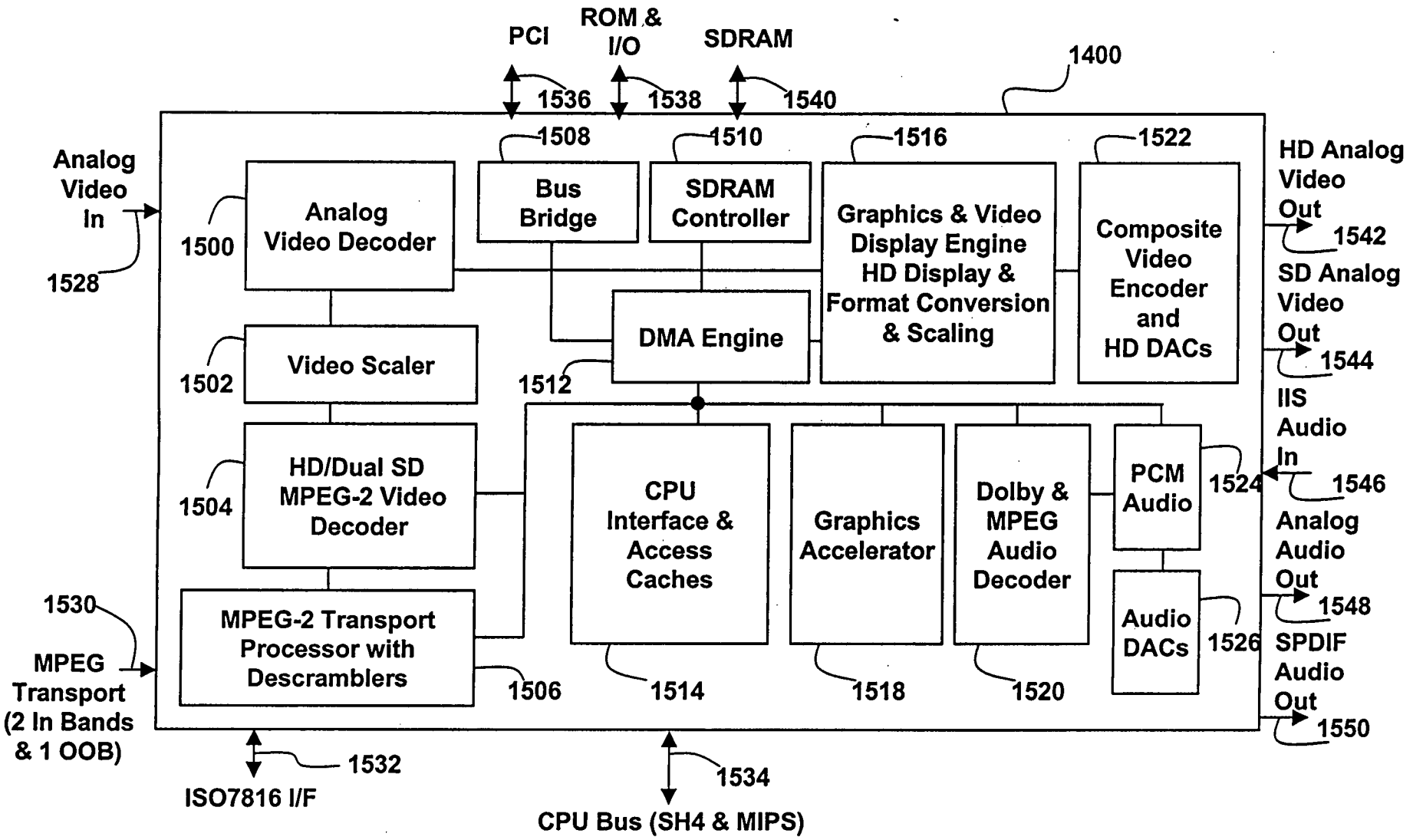
PCI
ROM & I/O
SDRAM
1536
1538
1540
1400
1508
1510
1516
1522
Analog Video In
1528
1500
Analog Video Decoder
Bus Bridge
SDRAM Controller
Graphics & Video Display Engine HD Display & Format Conversion & Scaling
Composite Video Encoder and HD DACs
HD Analog Video Out
1542
SD Analog Video Out
1544
DMA Engine
1502
Video Scaler
1512
IIS Audio In
1546
1504
HD/Dual SD MPEG-2 Video Decoder
CPU Interface & Access Caches
Graphics Accelerator
Dolby & MPEG Audio Decoder
PCM Audio
1524
Analog Audio Out
1548
1530
MPEG Transport (2 In Bands & 1 OOB)
MPEG-2 Transport Processor with Descramblers
1506
1514
1518
1520
Audio DACs
1526
SPDIF Audio Out
1550
1532
ISO7816 I/F
1534
CPU Bus (SH4 & MIPS)

FIG. 39

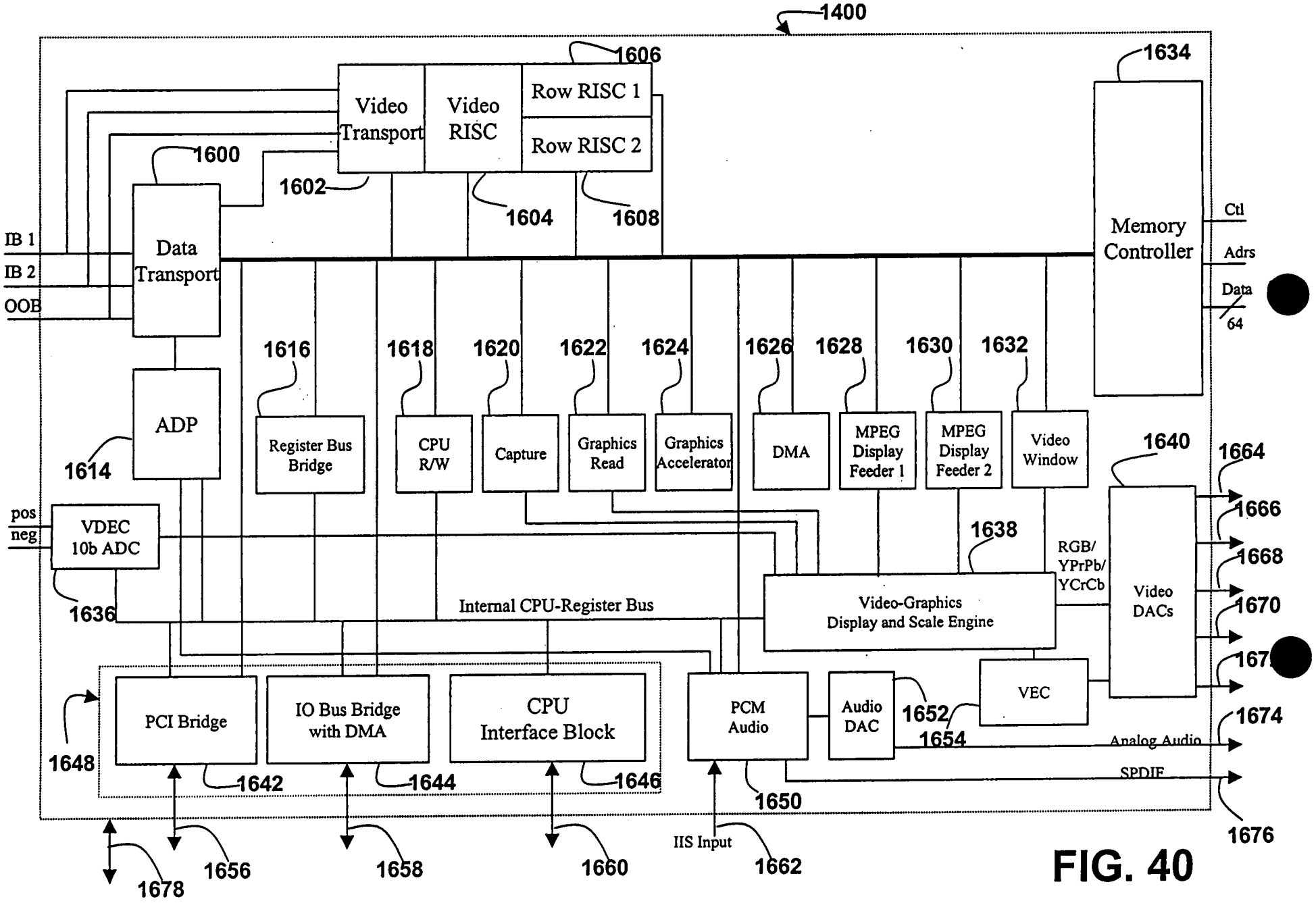
1400
1606
Video Transport
Video RISC
Row RISC 1
Row RISC 2
1634
Memory Controller
Ctl
Adrs
Data
64
1600
1602
1604
1608
IB 1
IB 2
OOB
Data Transport
1616
1618
1620
1622
1624
1626
1628
1630
1632
ADP
1614
Register Bus Bridge
CPU R/W
Capture
Graphics Read
Graphics Accelerator
DMA
MPEG Display Feeder 1
MPEG Display Feeder 2
Video Window
1640
1664
pos
neg
VDEC 10b ADC
1636
1638
RGB/ YPrPb/ YCrCb
Video DACs
1666
1668
1670
Internal CPU-Register Bus
Video-Graphics Display and Scale Engine
VEC
1652
1654
Audio DAC
PCM Audio
1674
Analog Audio
SPDIF
1676
1650
1648
PCI Bridge
IO Bus Bridge with DMA
CPU Interface Block
1642
1644
1646
IIS Input
1662
1678
1656
1658
1660

FIG. 40

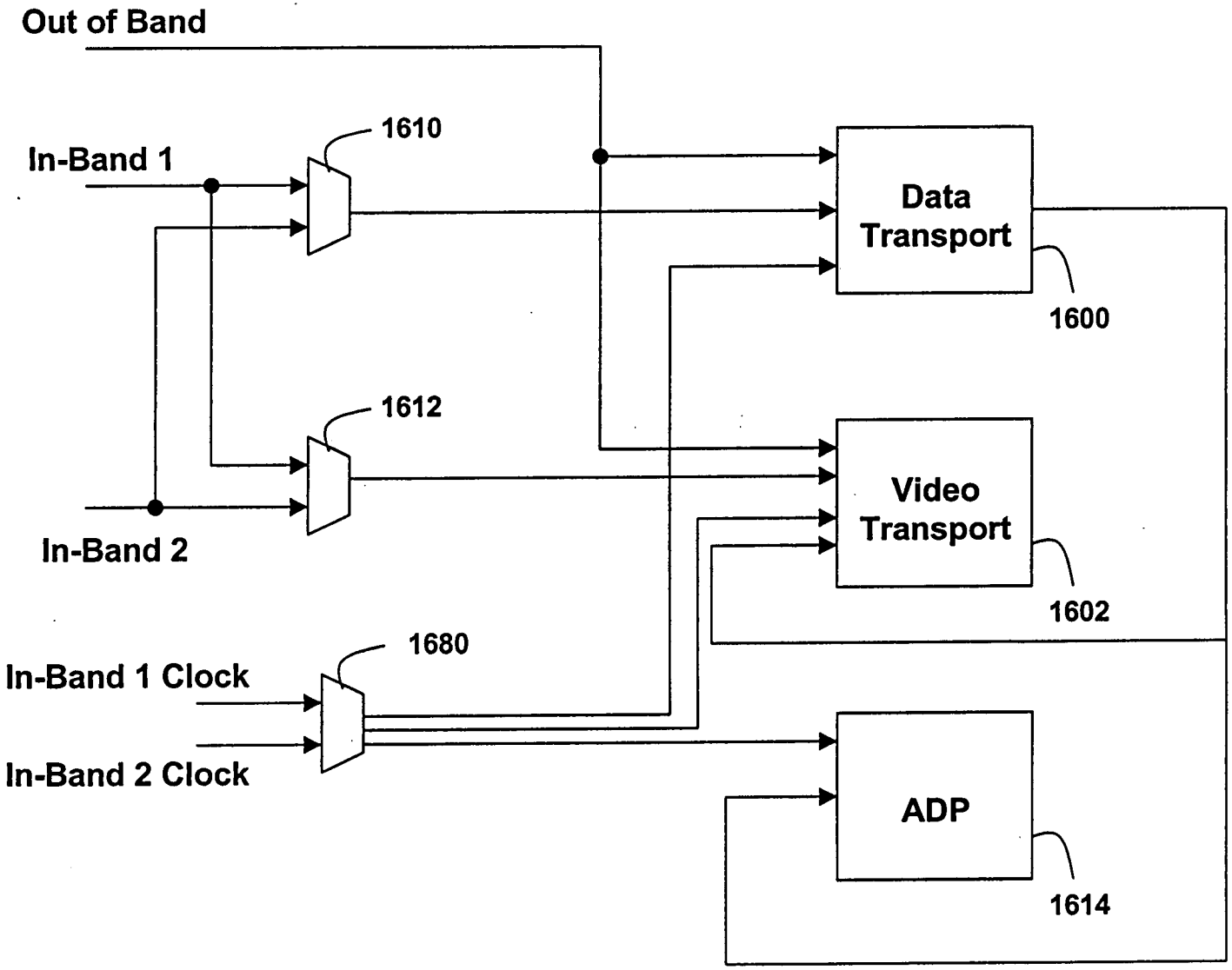

FIG. 41

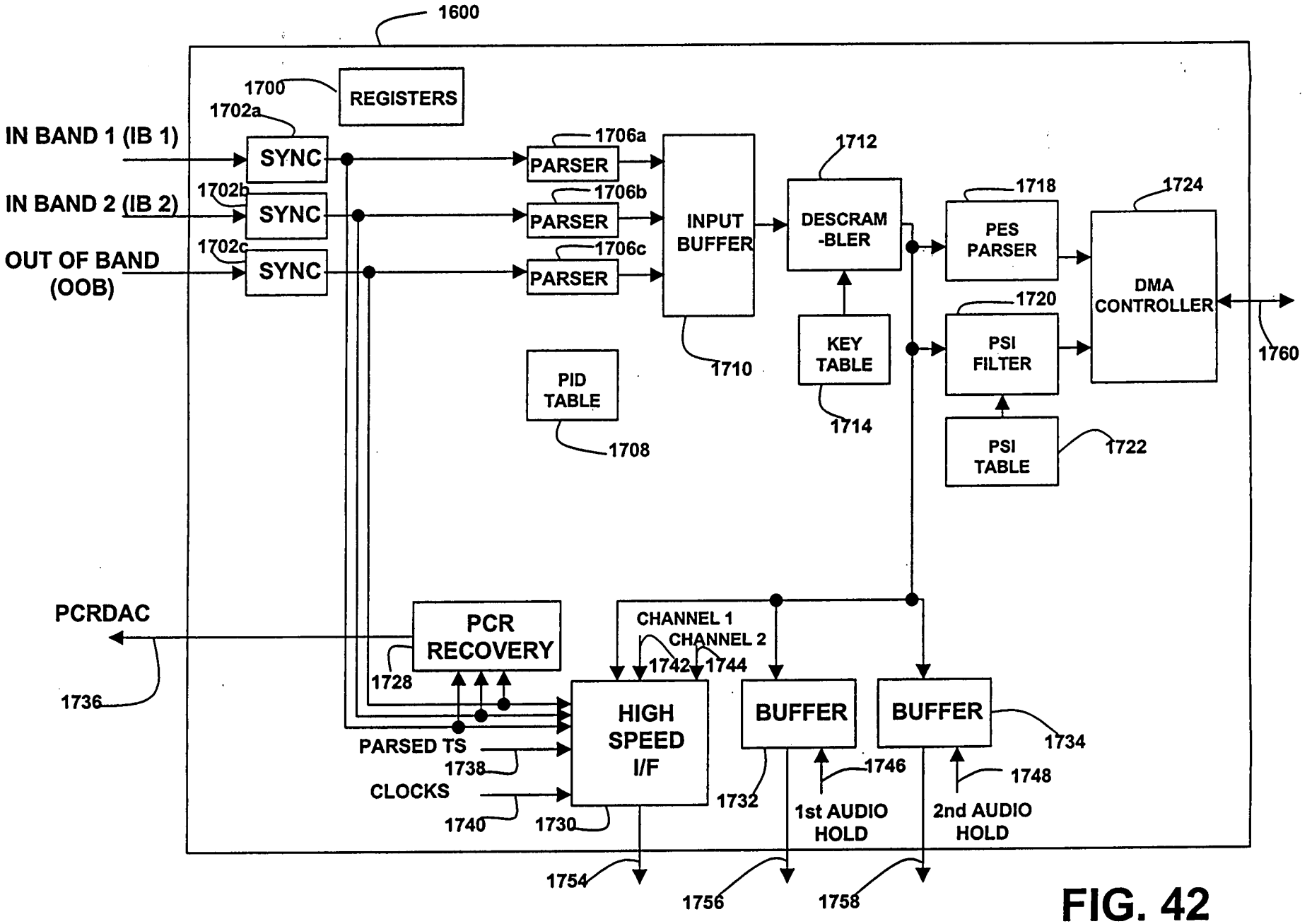

FIG. 42

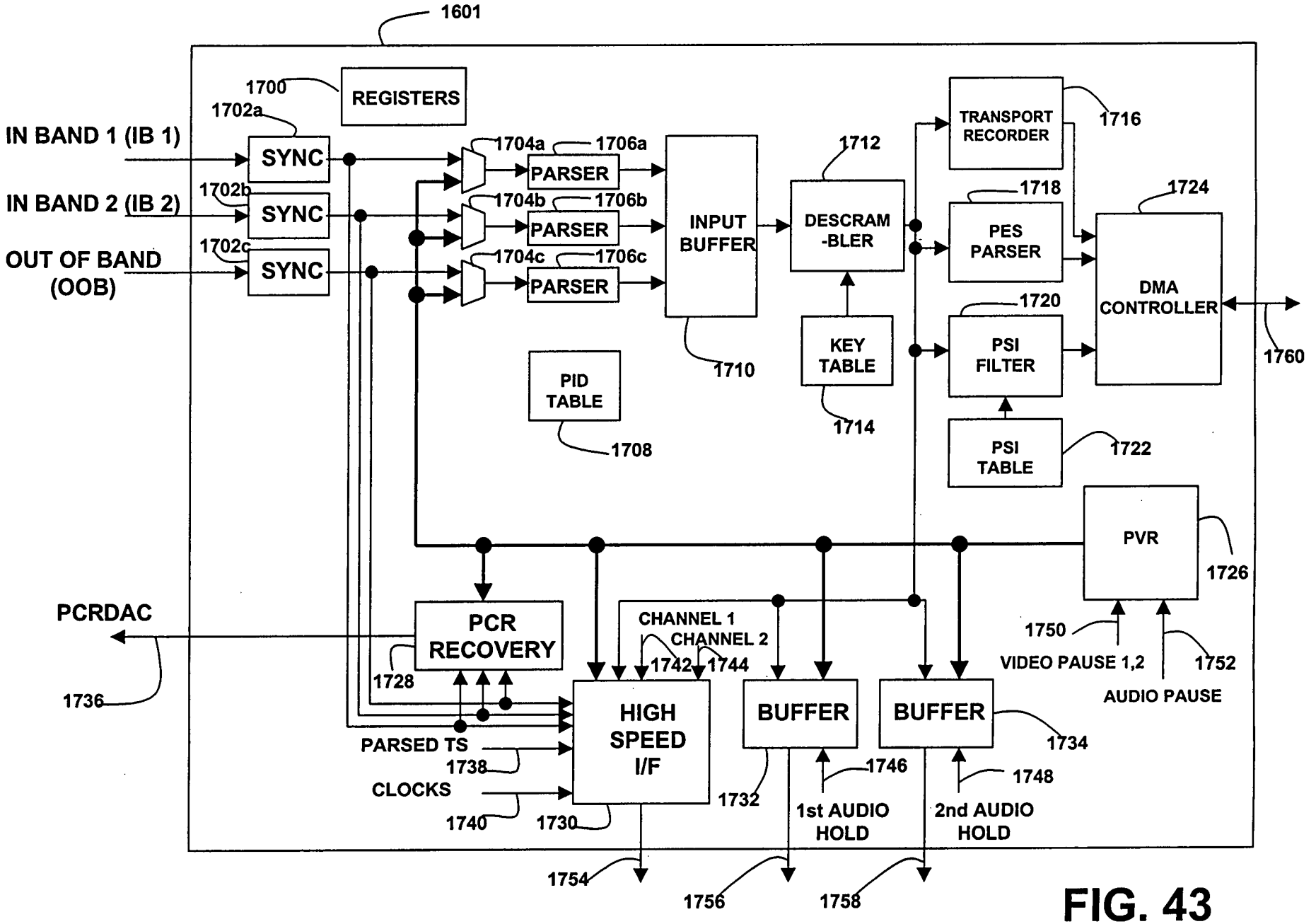
1601
1700
REGISTERS
1702a
IN BAND 1 (IB 1)
SYNC
1702b
IN BAND 2 (IB 2)
SYNC
1702c
OUT OF BAND (OOB)
SYNC
1704a
1706a
PARSER
1704b
1706b
PARSER
1704c
1706c
PARSER
INPUT BUFFER
1710
1712
DESCRAM -BLER
KEY TABLE
1714
PID TABLE
1708
TRANSPORT RECORDER
1716
1718
PES PARSER
1720
PSI FILTER
PSI TABLE
1722
1724
DMA CONTROLLER
1760
PVR
1726
PCRDAC
1736
PCR RECOVERY
1728
CHANNEL 1
CHANNEL 2
1742
1744
1750
VIDEO PAUSE 1,2
1752
AUDIO PAUSE
PARSED TS
1738
CLOCKS
1740
HIGH SPEED I/F
1730
1732
BUFFER
BUFFER
1734
1746
1748
1st AUDIO HOLD
2nd AUDIO HOLD
1754
1756
1758

FIG. 43

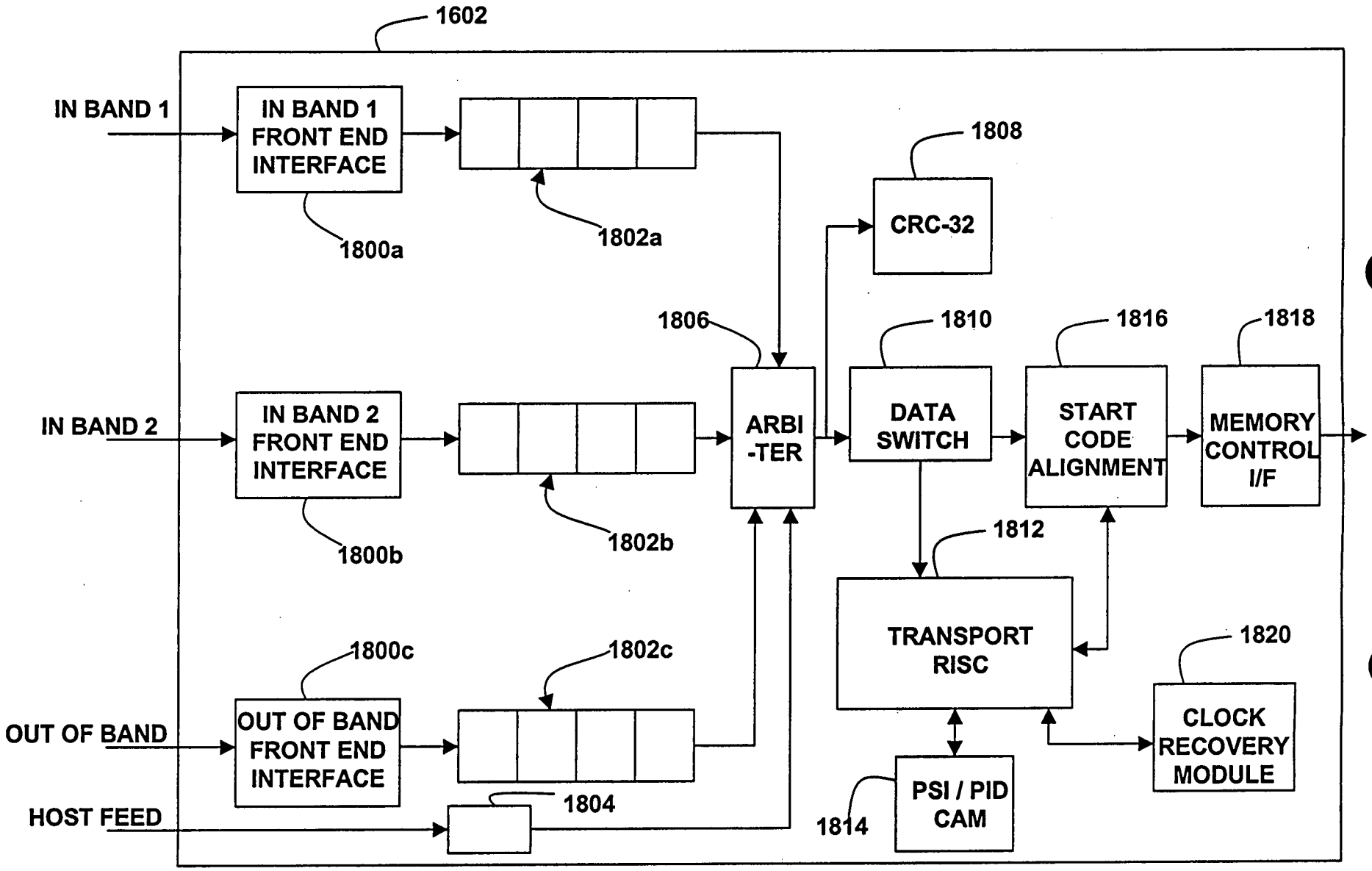
1602
IN BAND 1
IN BAND 1 FRONT END INTERFACE
1800a
1802a
1808
CRC-32
1806
1810
1816
1818
IN BAND 2
IN BAND 2 FRONT END INTERFACE
1800b
1802b
ARBI -TER
DATA SWITCH
START CODE ALIGNMENT
MEMORY CONTROL I/F
1812
TRANSPORT RISC
1820
1800c
1802c
OUT OF BAND
OUT OF BAND FRONT END INTERFACE
CLOCK RECOVERY MODULE
1804
HOST FEED
1814
PSI / PID CAM

FIG. 44

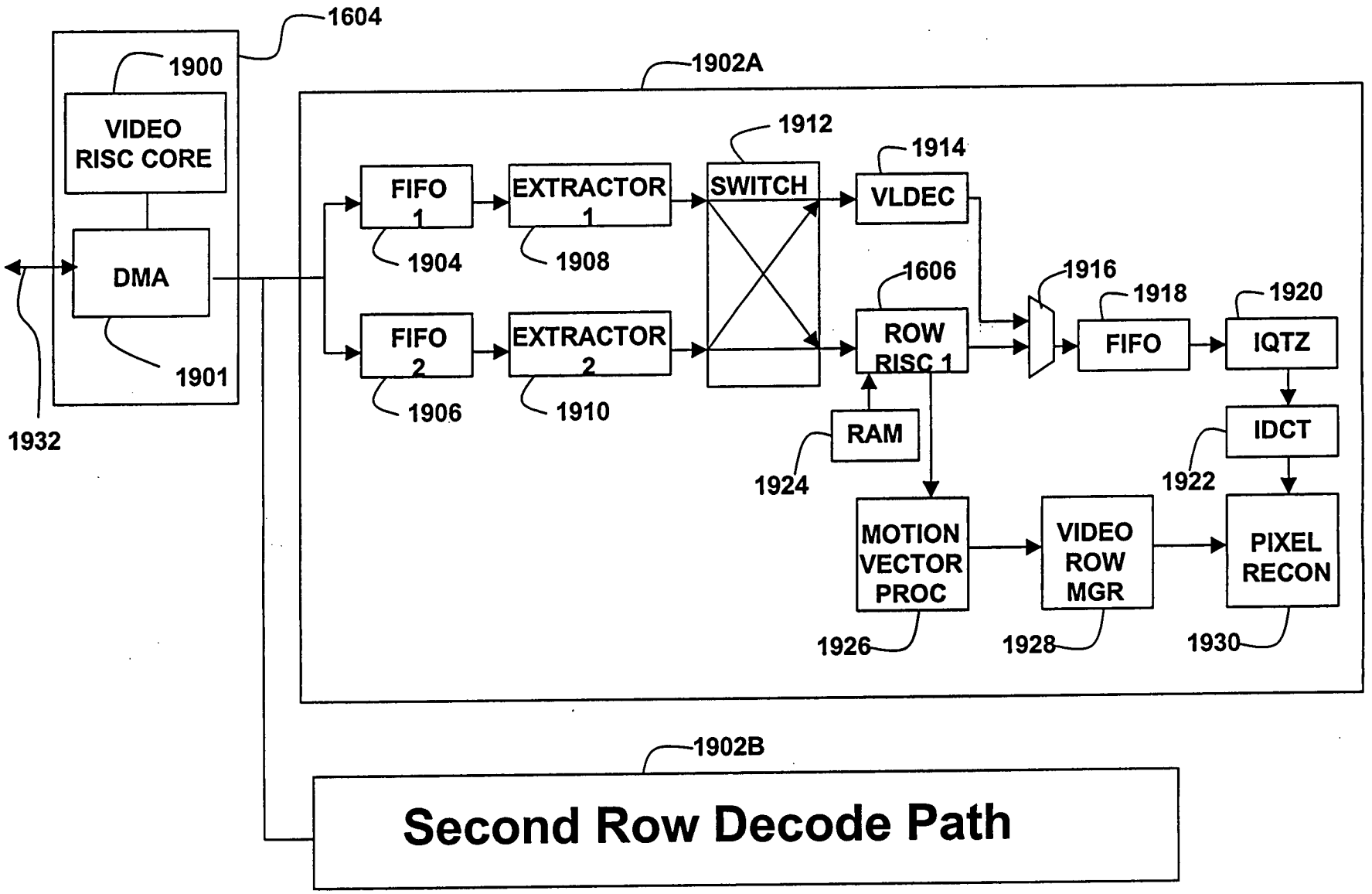

FIG. 45

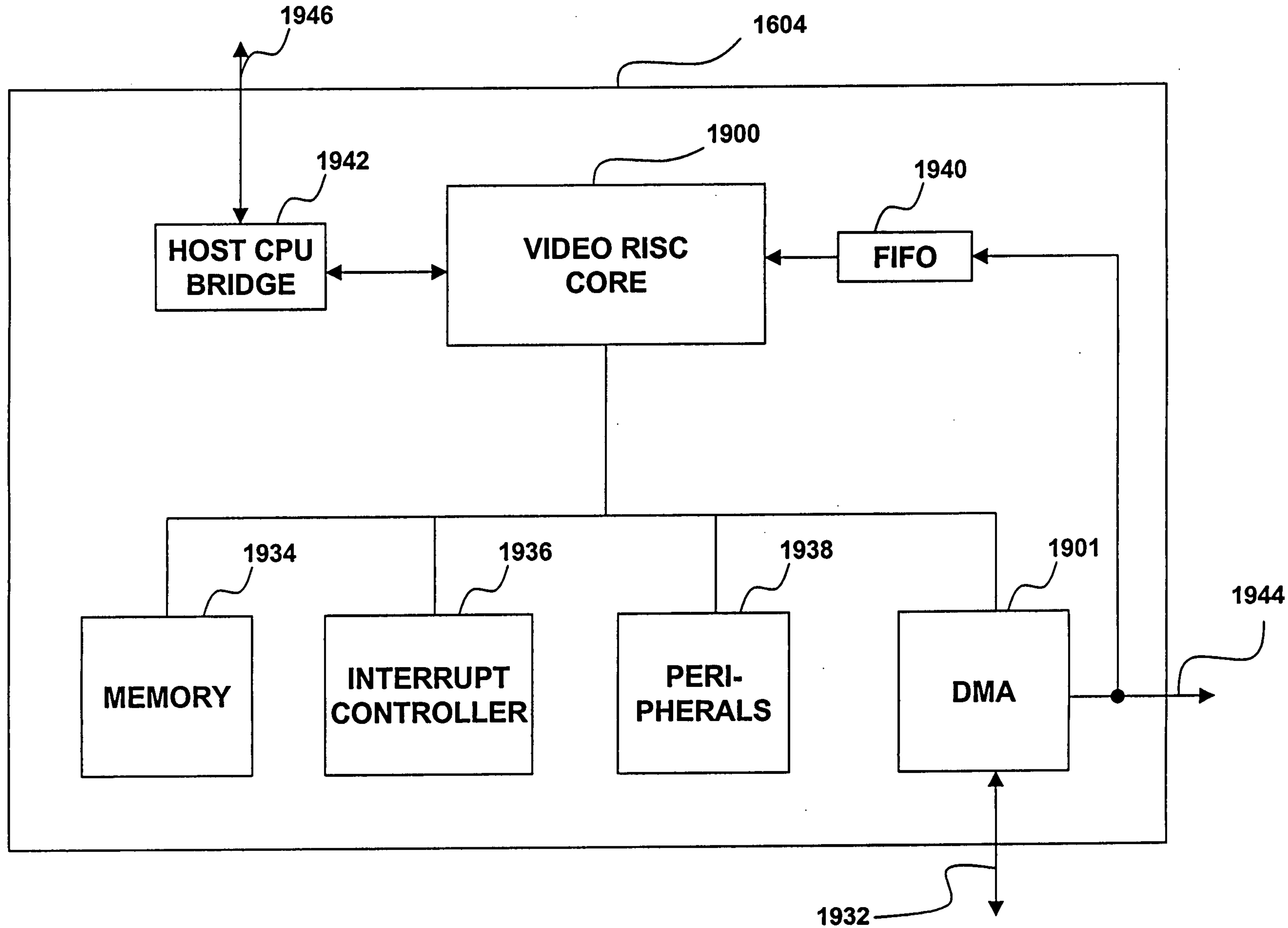

FIG. 46

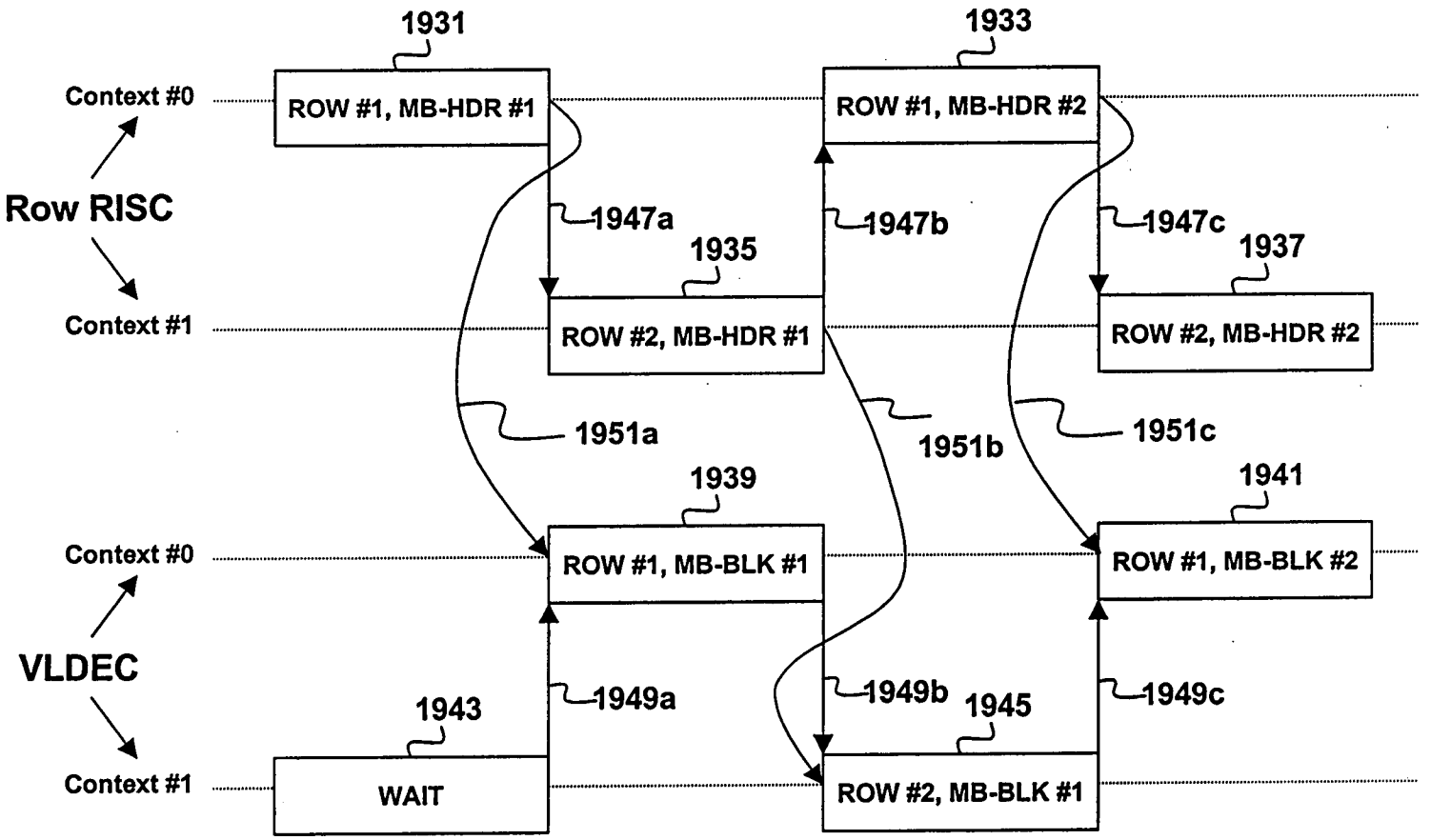
1931
1933
Context #0
ROW #1, MB-HDR #1
ROW #1, MB-HDR #2
Row RISC
1947a
1947b
1947c
1935
1937
Context #1
ROW #2, MB-HDR #1
ROW #2, MB-HDR #2
1951a
1951b
1951c
1939
1941
Context #0
ROW #1, MB-BLK #1
ROW #1, MB-BLK #2
VLDEC
1949a
1949b
1949c
1943
1945
Context #1
WAIT
ROW #2, MB-BLK #1

FIG. 47

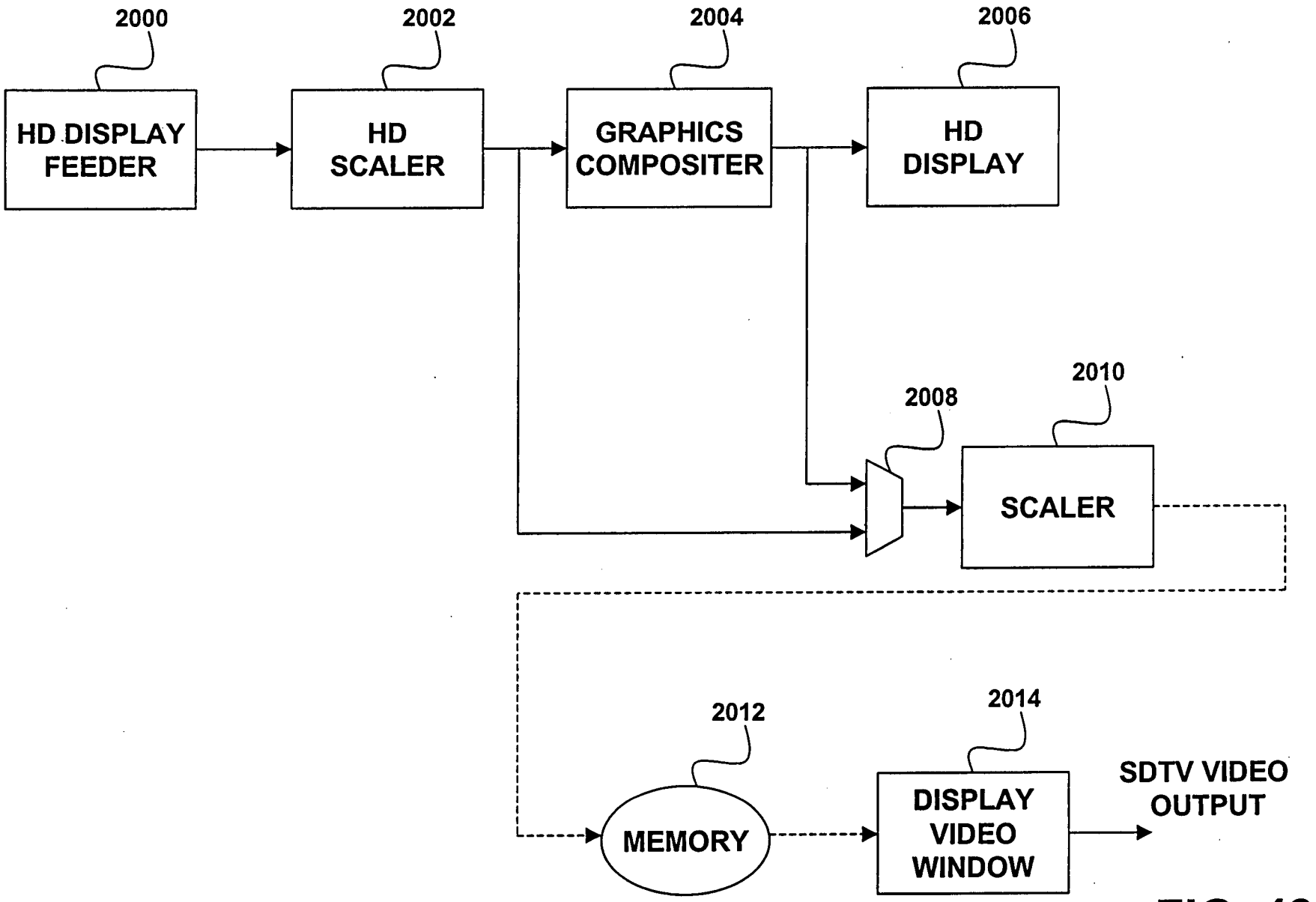

FIG. 48

MPEG VIDEO DECODING STAGES

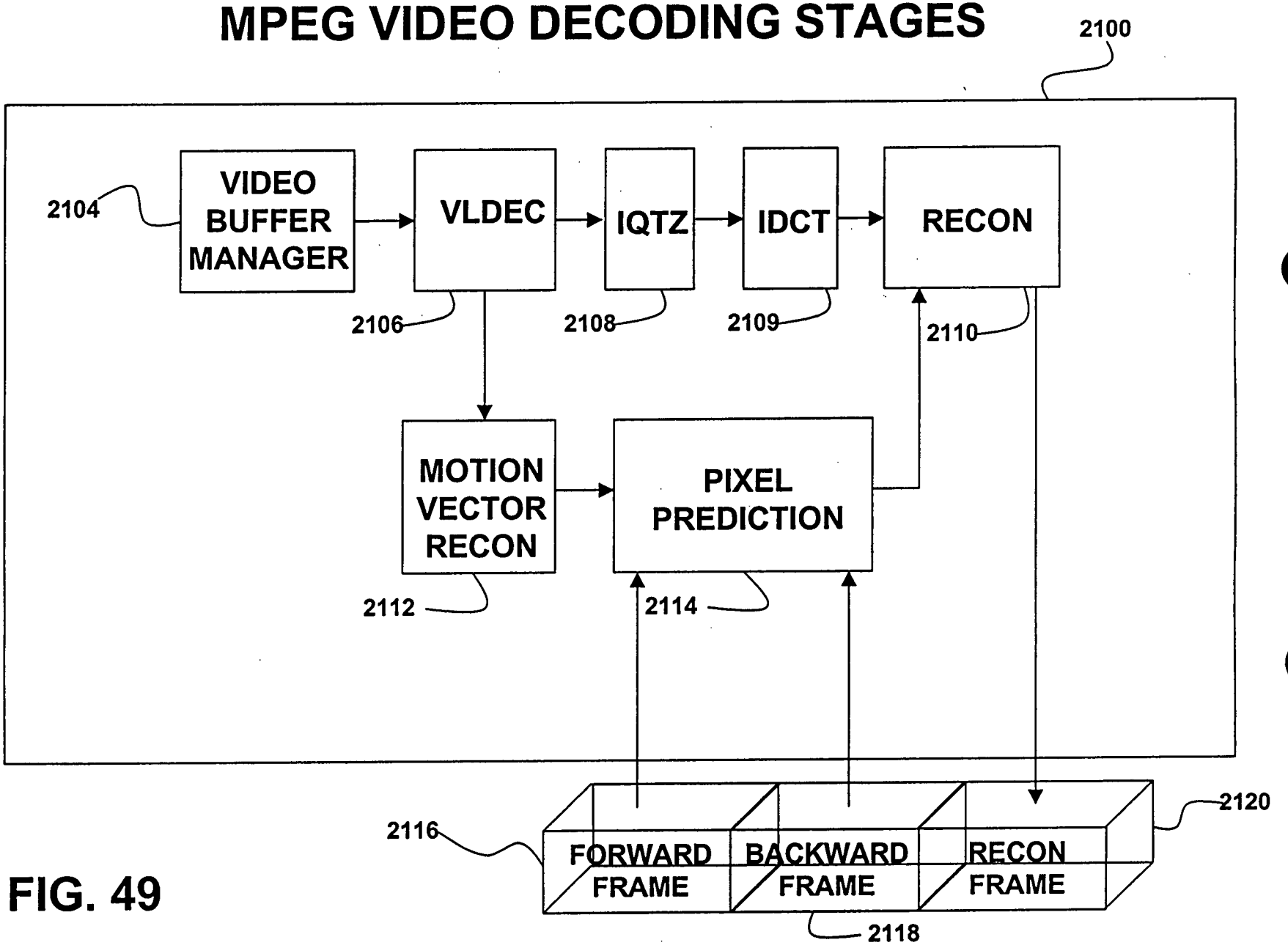

FIG. 49

MPEG VIDEO DECODING STAGES WITH VIDEO TIME DOWNSCALING

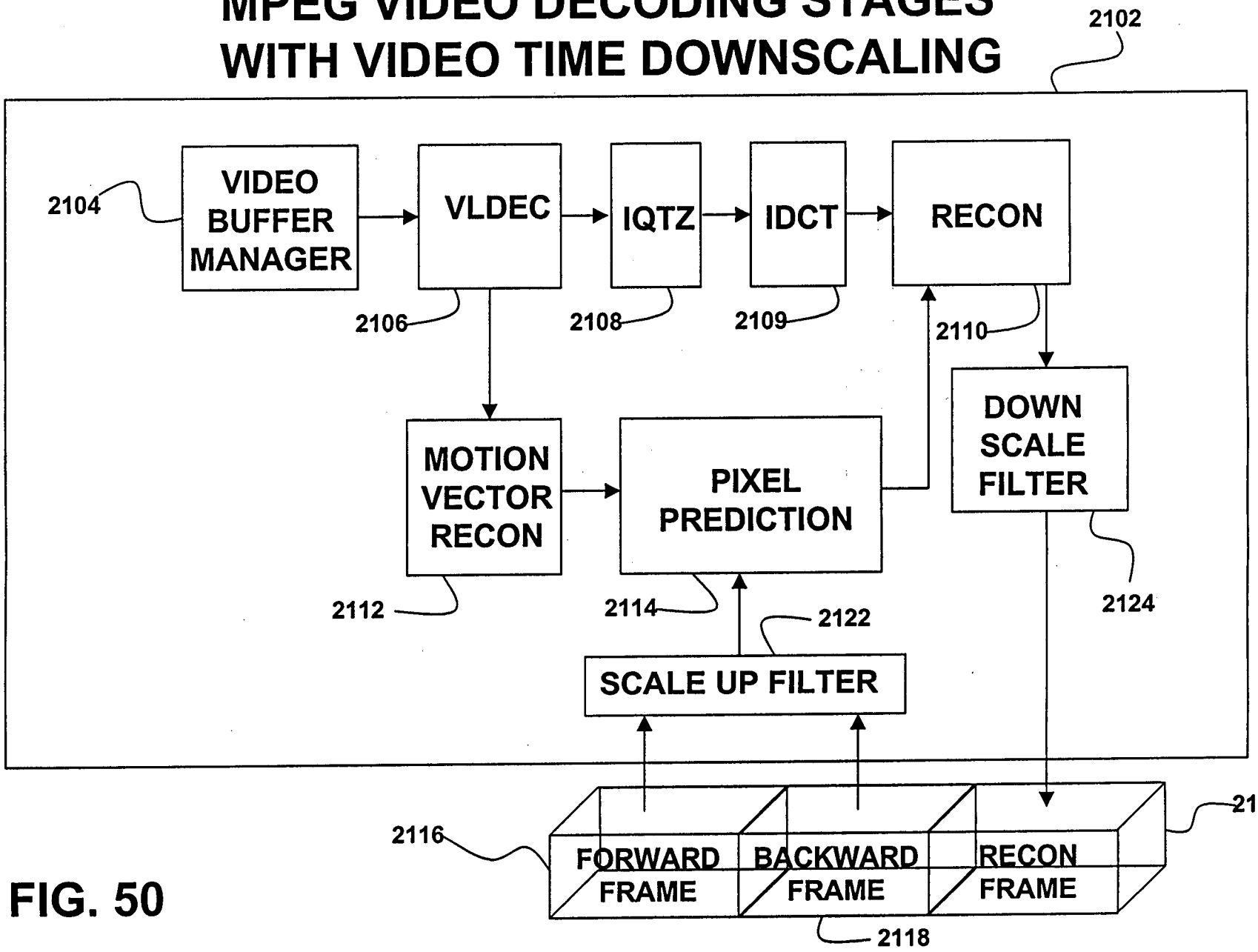

FIG. 50

FRAME-PREDICTION FOR I-PICTURES AND P-PICTURES

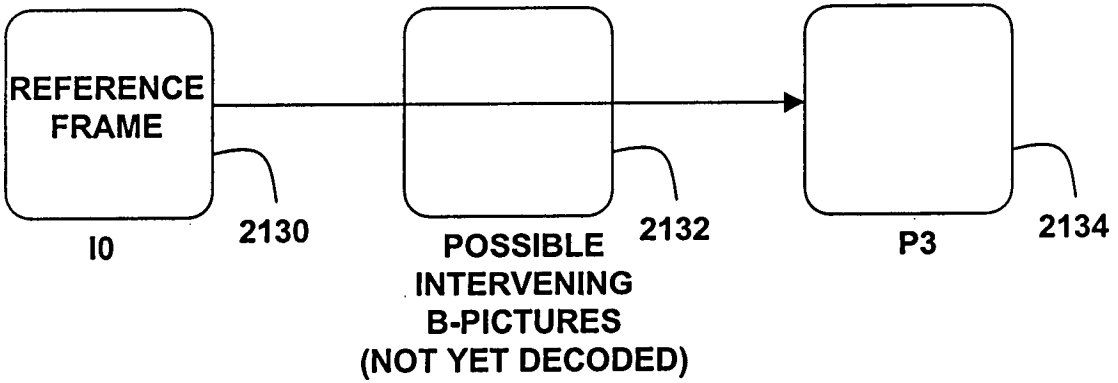

FIG. 51

FIELD PREDICTION IN A FRAME-PICTURE

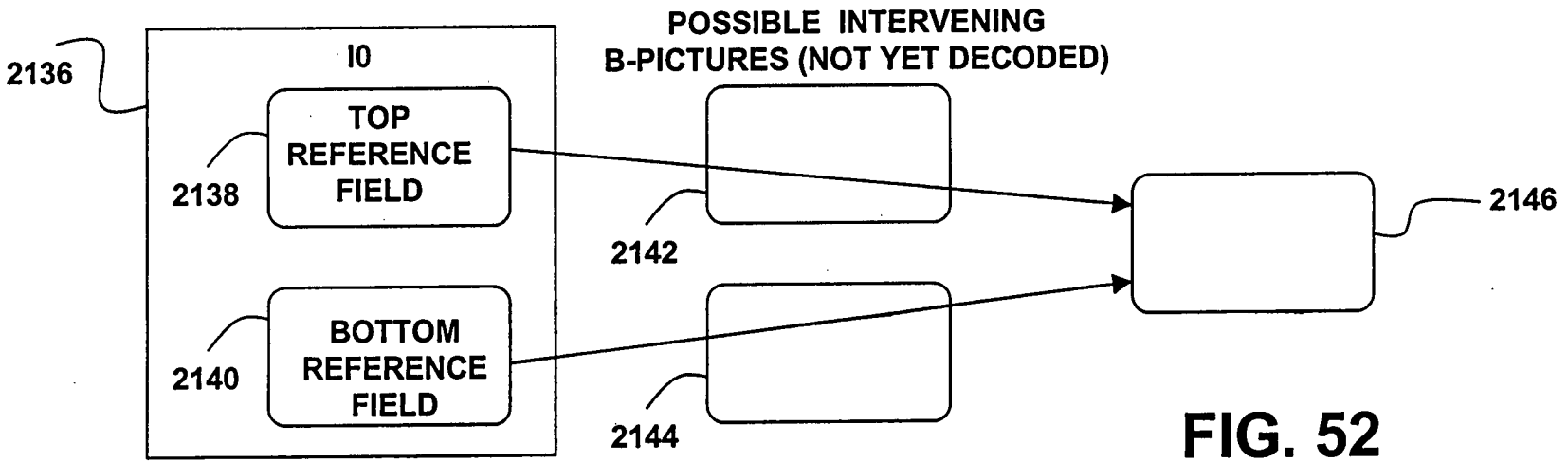

FIG. 52

PREDICTION OF THE FIRST FIELD-PICTURE

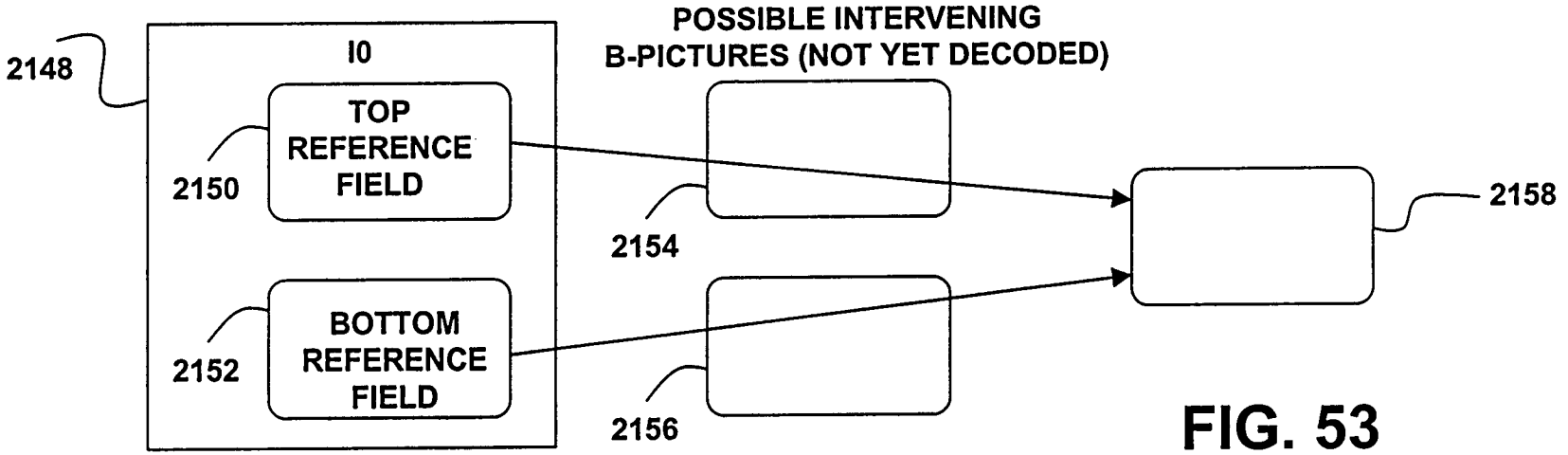

FIG. 53

PREDICTION OF THE "BOTTOM FIELD" SECOND FIELD-PICTURE

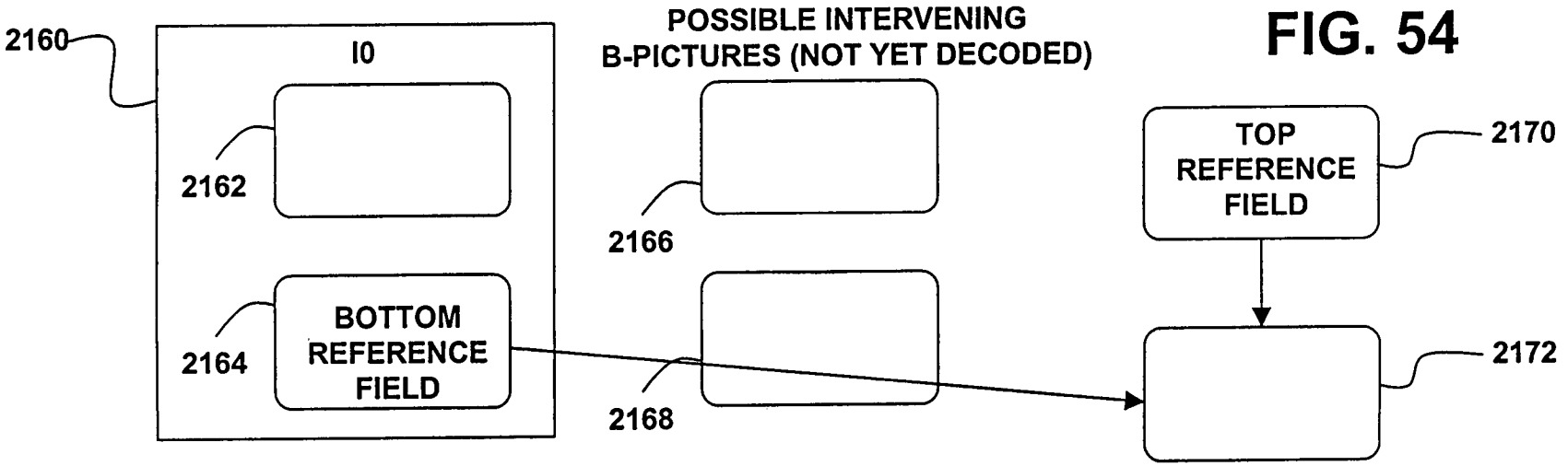

FIG. 54

PREDICTION OF THE "TOP FIELD" SECOND FIELD-PICTURE

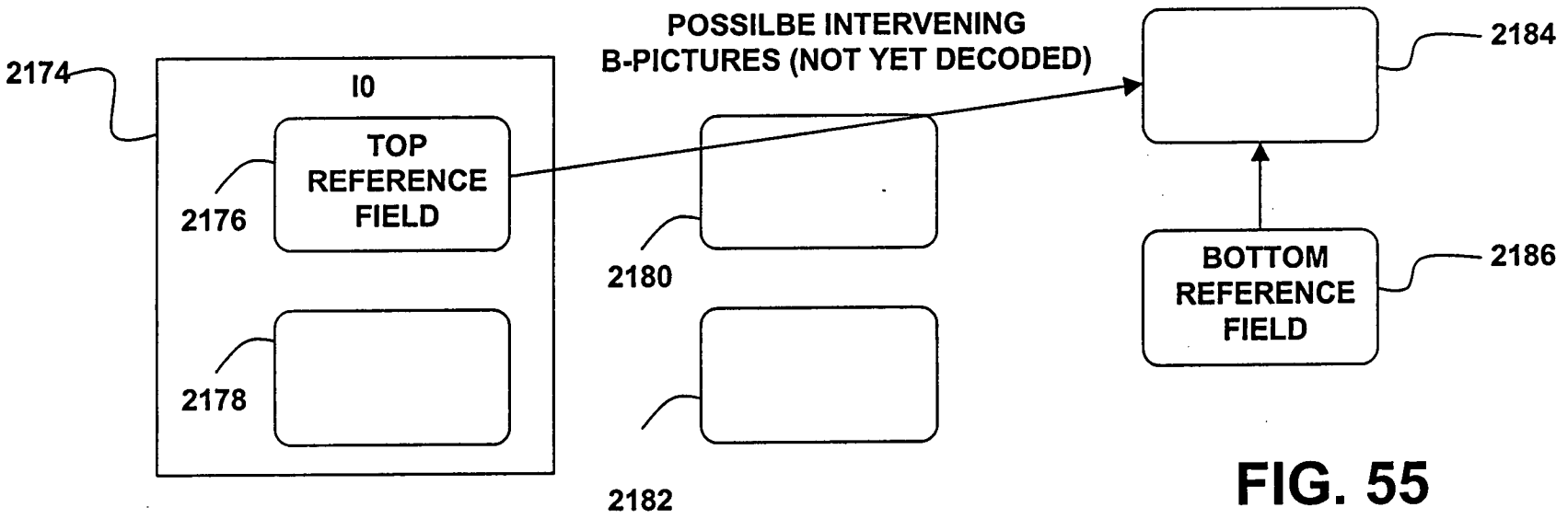

FIG. 55

FIELD-PREDICTIONOF B FIELD PICTURES OR B FRAME PICTURES

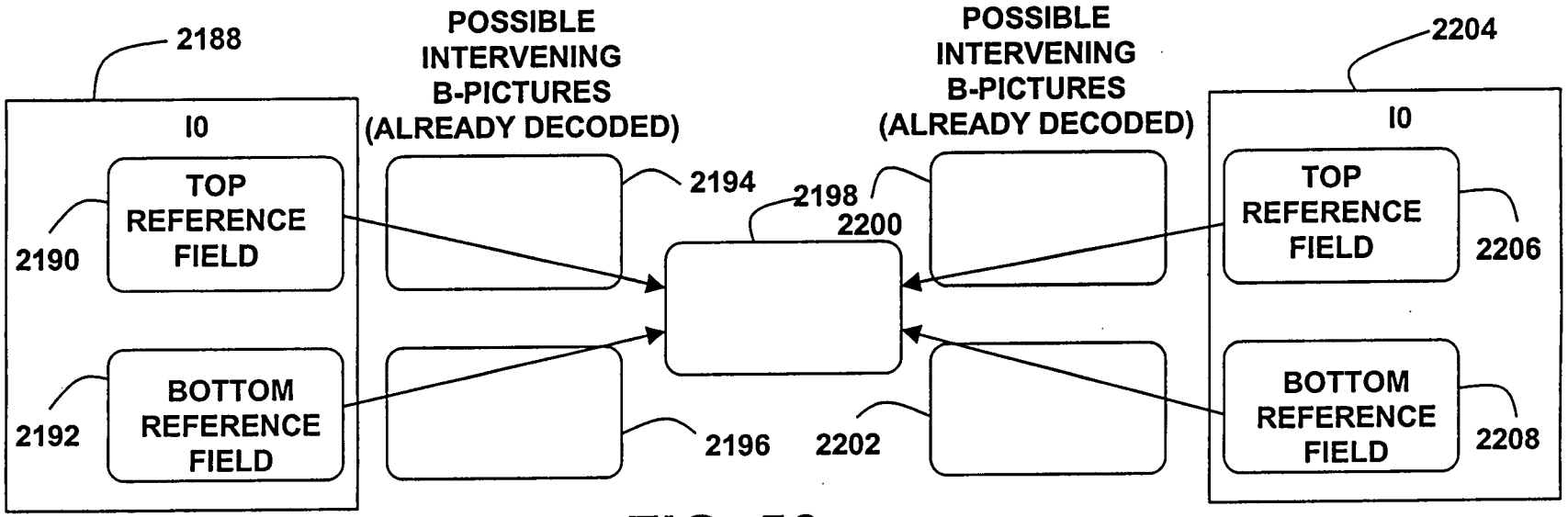

FIG. 56

FRAME-PREDICTIONS FOR B-PICTURES

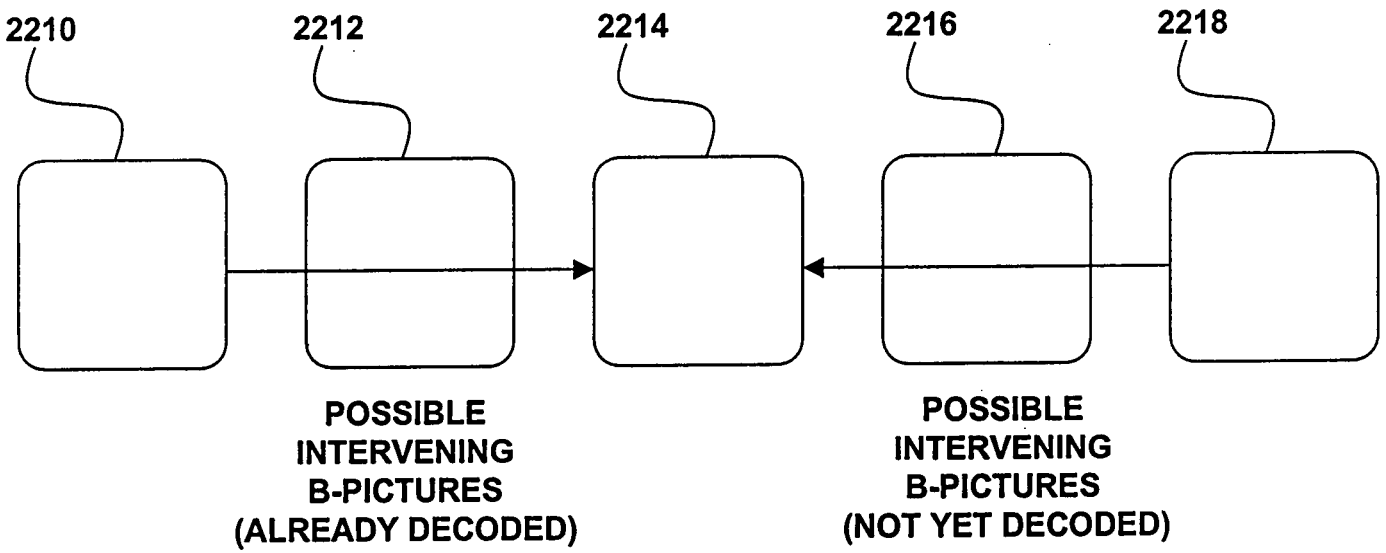

FIG. 57

Image Organization - 64 bit SDRAM

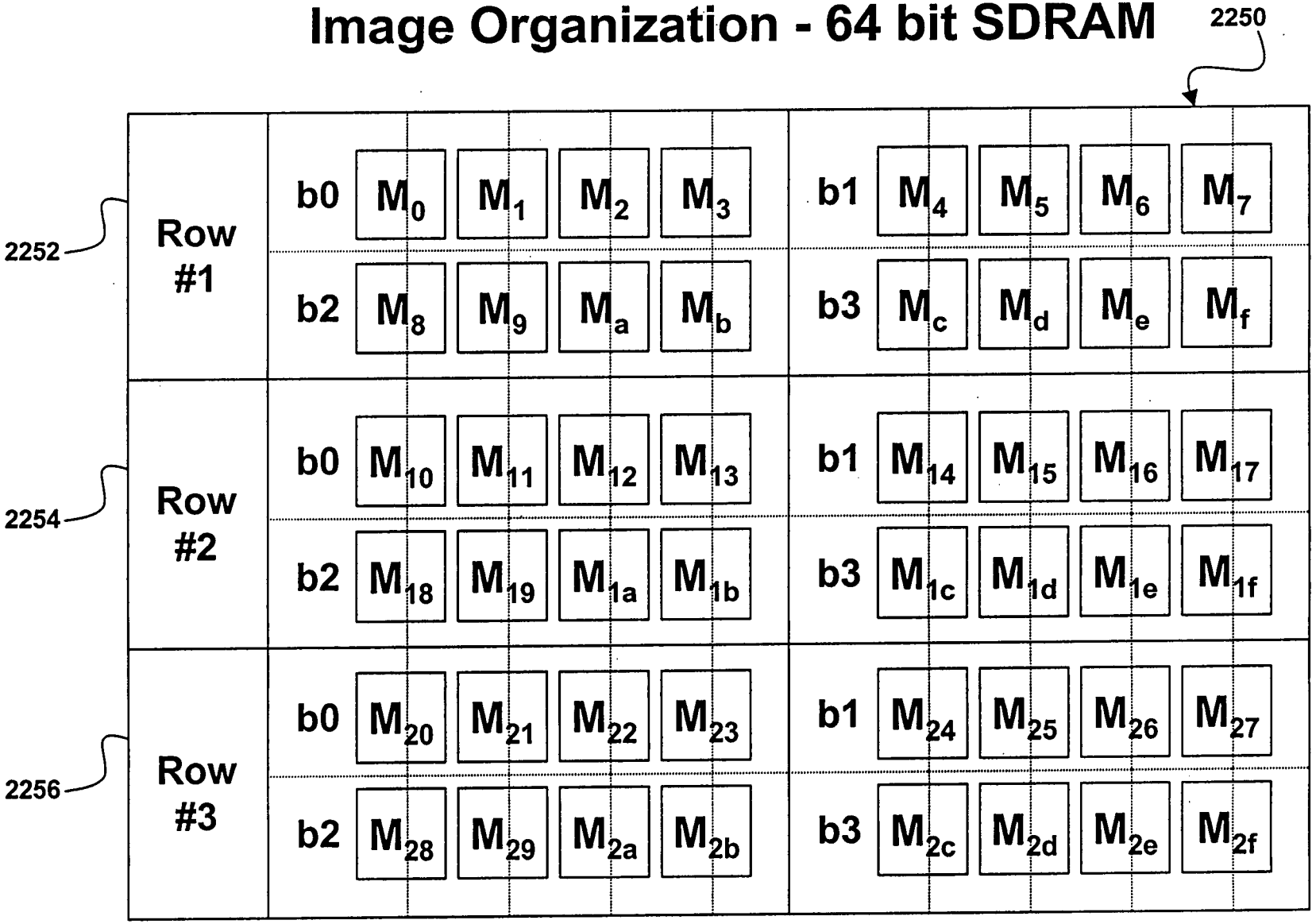

FIG. 58

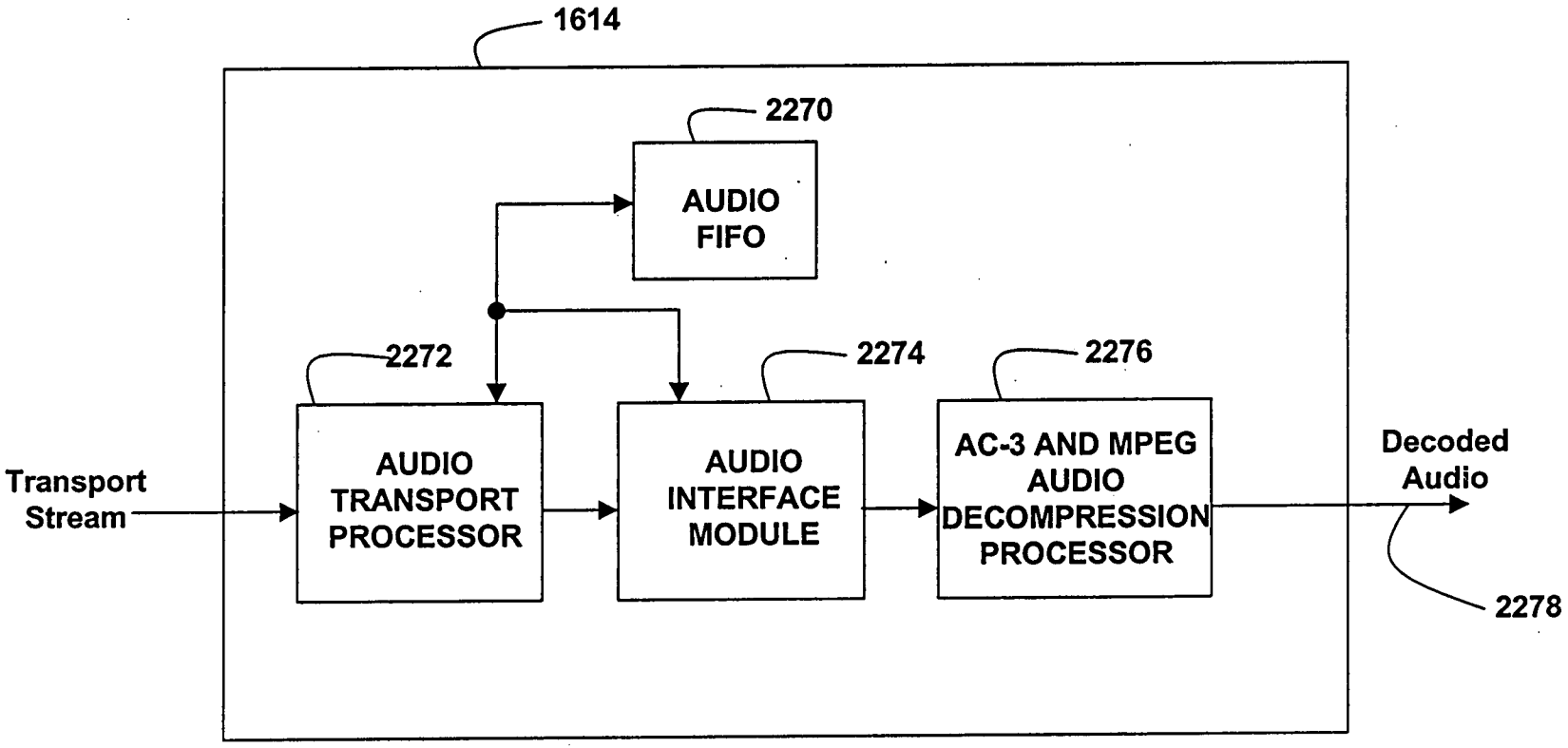
1614
2270
AUDIO FIFO
2272
2274
2276
Transport Stream
AUDIO TRANSPORT PROCESSOR
AUDIO INTERFACE MODULE
AC-3 AND MPEG AUDIO DECOMPRESSION PROCESSOR
Decoded Audio
2278

FIG. 59

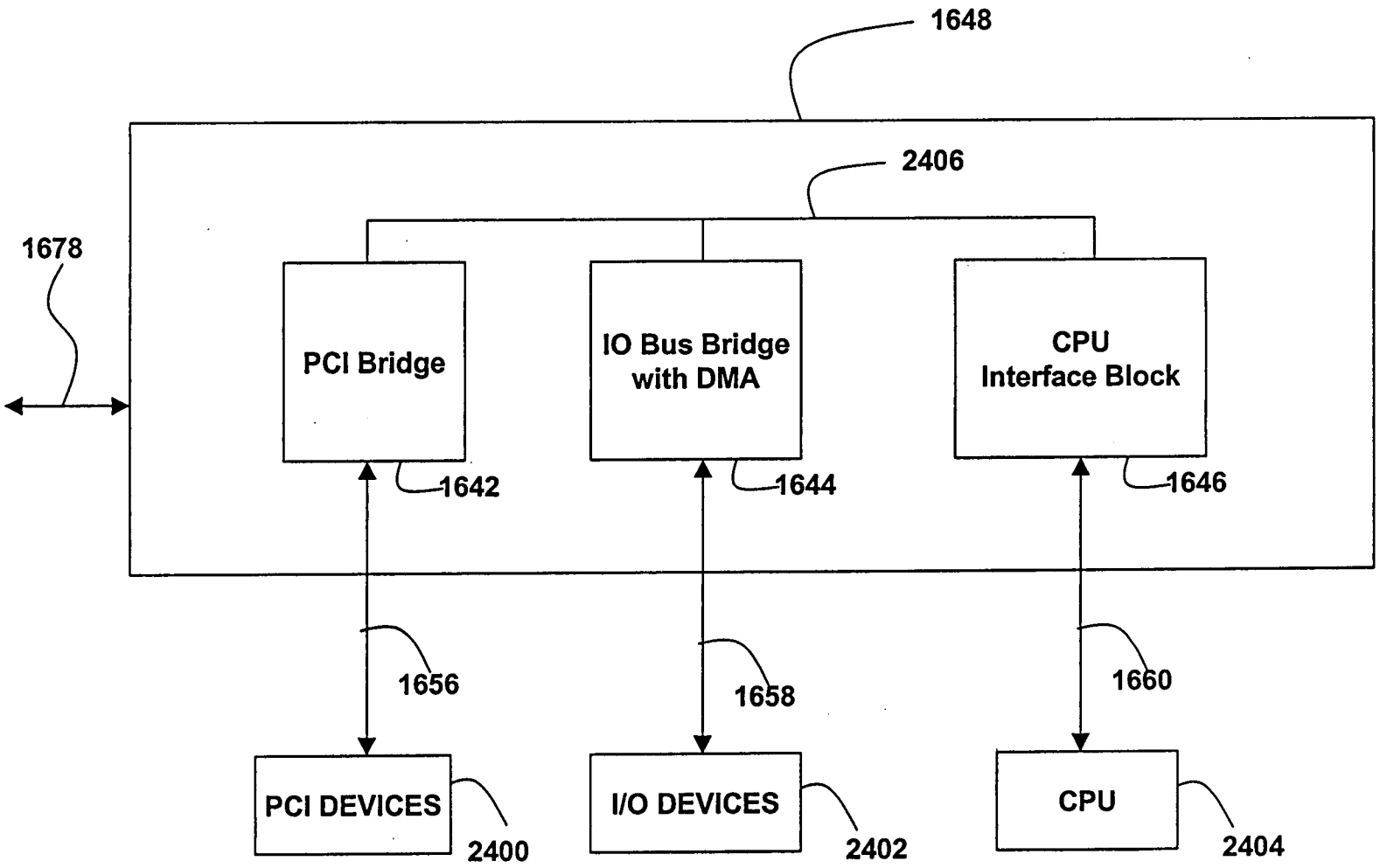
1648
2406
1678
PCI Bridge
IO Bus Bridge with DMA
CPU Interface Block
1642
1644
1646
1656
1658
1660
PCI DEVICES
2400
I/O DEVICES
2402
CPU
2404

FIG. 60

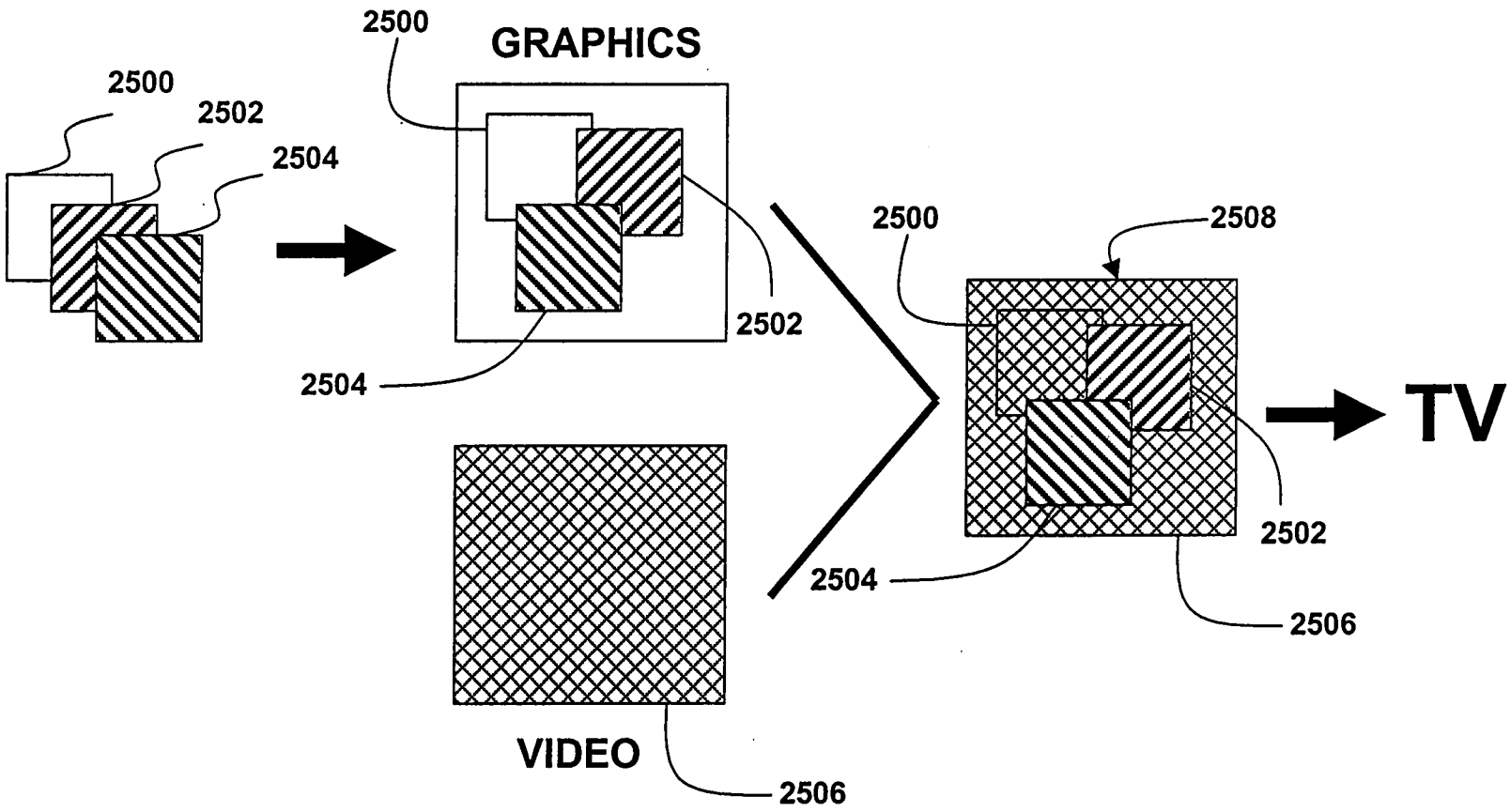

FIG. 61

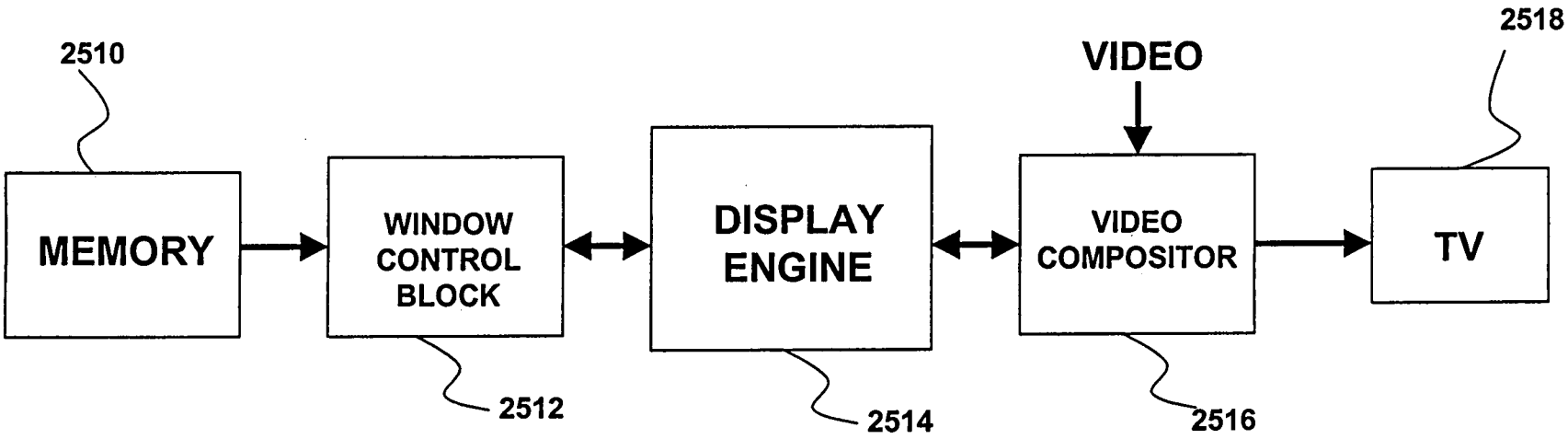

FIG. 62

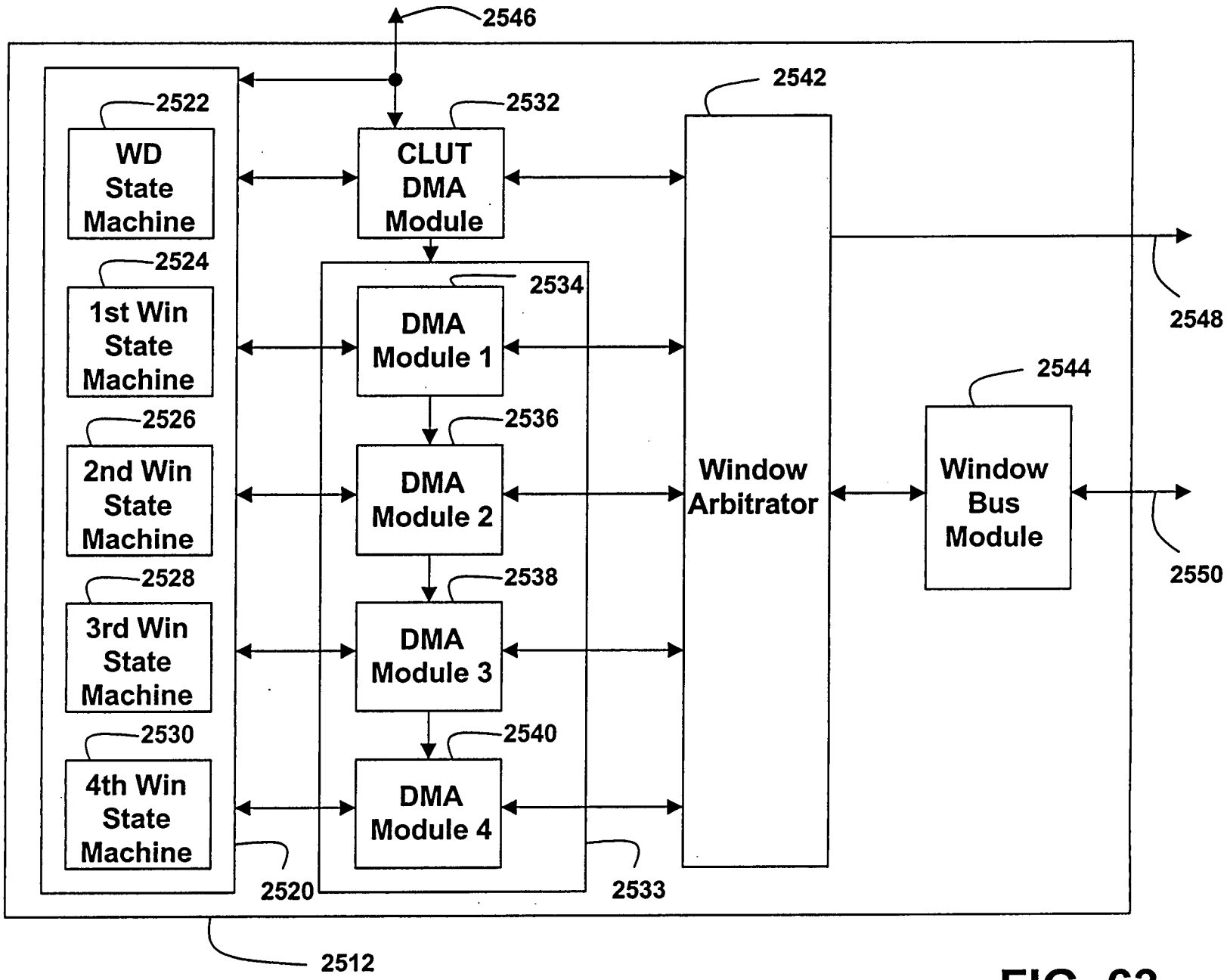
2546
2522
WD State Machine
2524
1st Win State Machine
2526
2nd Win State Machine
2528
3rd Win State Machine
2530
4th Win State Machine
2532
CLUT DMA Module
2534
DMA Module 1
2536
DMA Module 2
2538
DMA Module 3
2540
DMA Module 4
2542
Window Arbitrator
2544
Window Bus Module
2548
2550
2520
2533
2512

FIG. 63

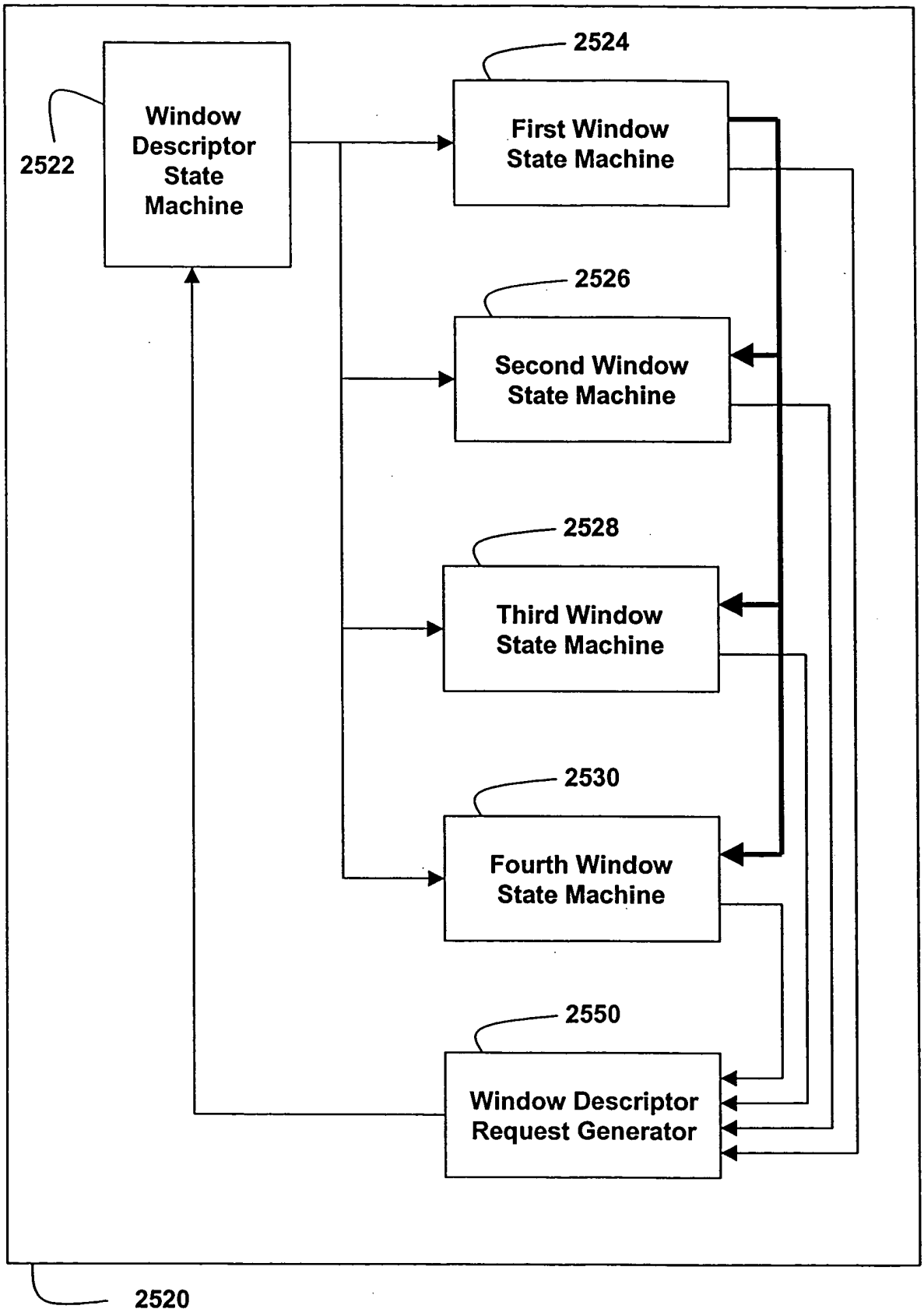
2524
Window Descriptor State Machine
2522
First Window State Machine
2526
Second Window State Machine
2528
Third Window State Machine
2530
Fourth Window State Machine
2550
Window Descriptor Request Generator
2520

FIG. 64

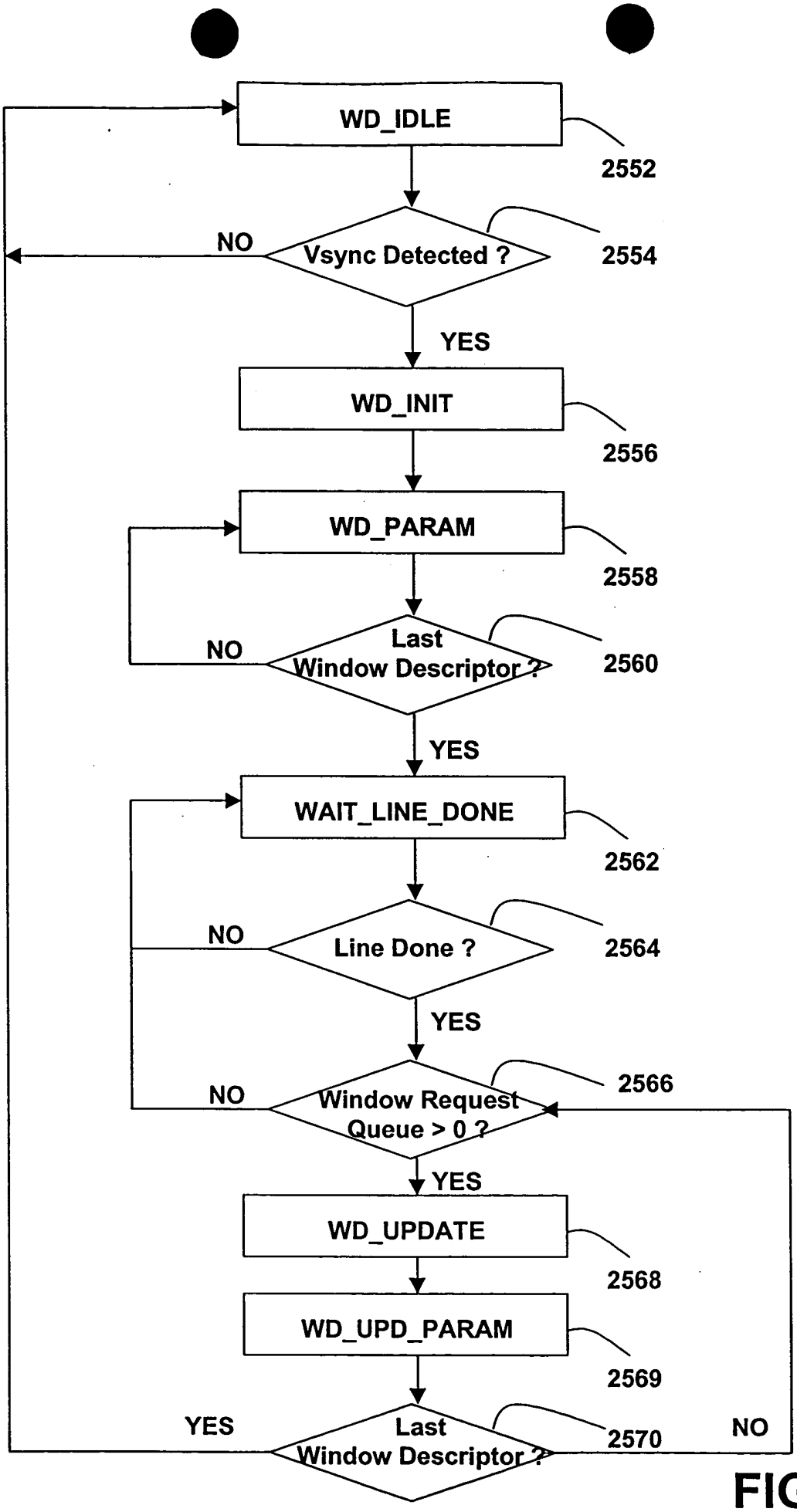
WD_IDLE
2552
Vsync Detected ?
NO
2554
YES
WD_INIT
2556
WD_PARAM
2558
Last
Window Descriptor ?
NO
2560
YES
WAIT_LINE_DONE
2562
Line Done ?
NO
2564
YES
Window Request
Queue > 0 ?
NO
2566
YES
WD_UPDATE
2568
WD_UPD_PARAM
2569
Last
Window Descriptor ?
YES
2570
NO

FIG. 65

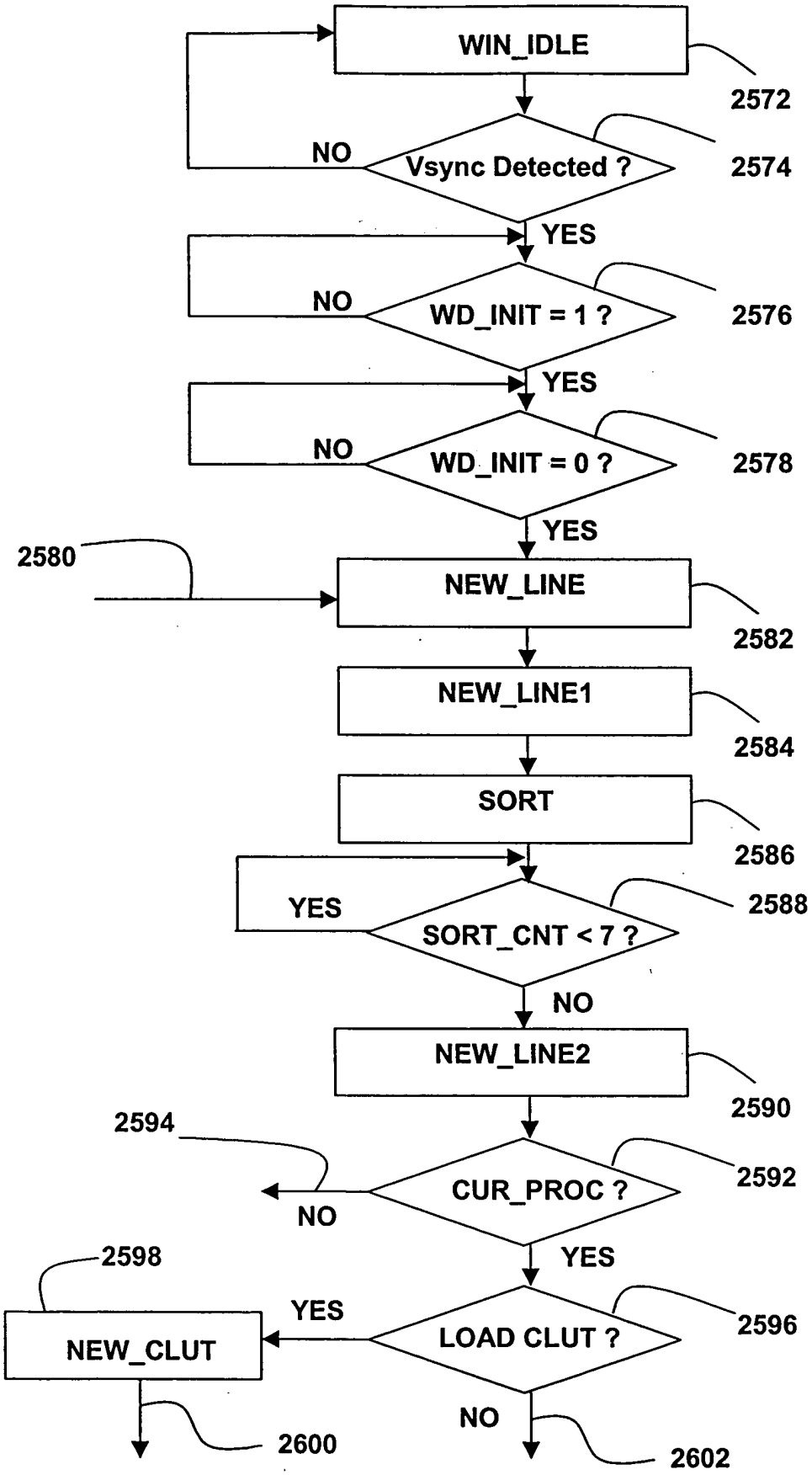
WIN_IDLE
2572
NO
Vsync Detected ?
2574
YES
NO
WD_INIT = 1 ?
2576
YES
NO
WD_INIT = 0 ?
2578
YES
2580
NEW_LINE
2582
NEW_LINE1
2584
SORT
2586
YES
SORT_CNT < 7 ?
2588
NO
NEW_LINE2
2590
2594
NO
CUR_PROC ?
2592
YES
2598
YES
NEW_CLUT
LOAD CLUT ?
2596
NO
2600
2602

FIG. 66

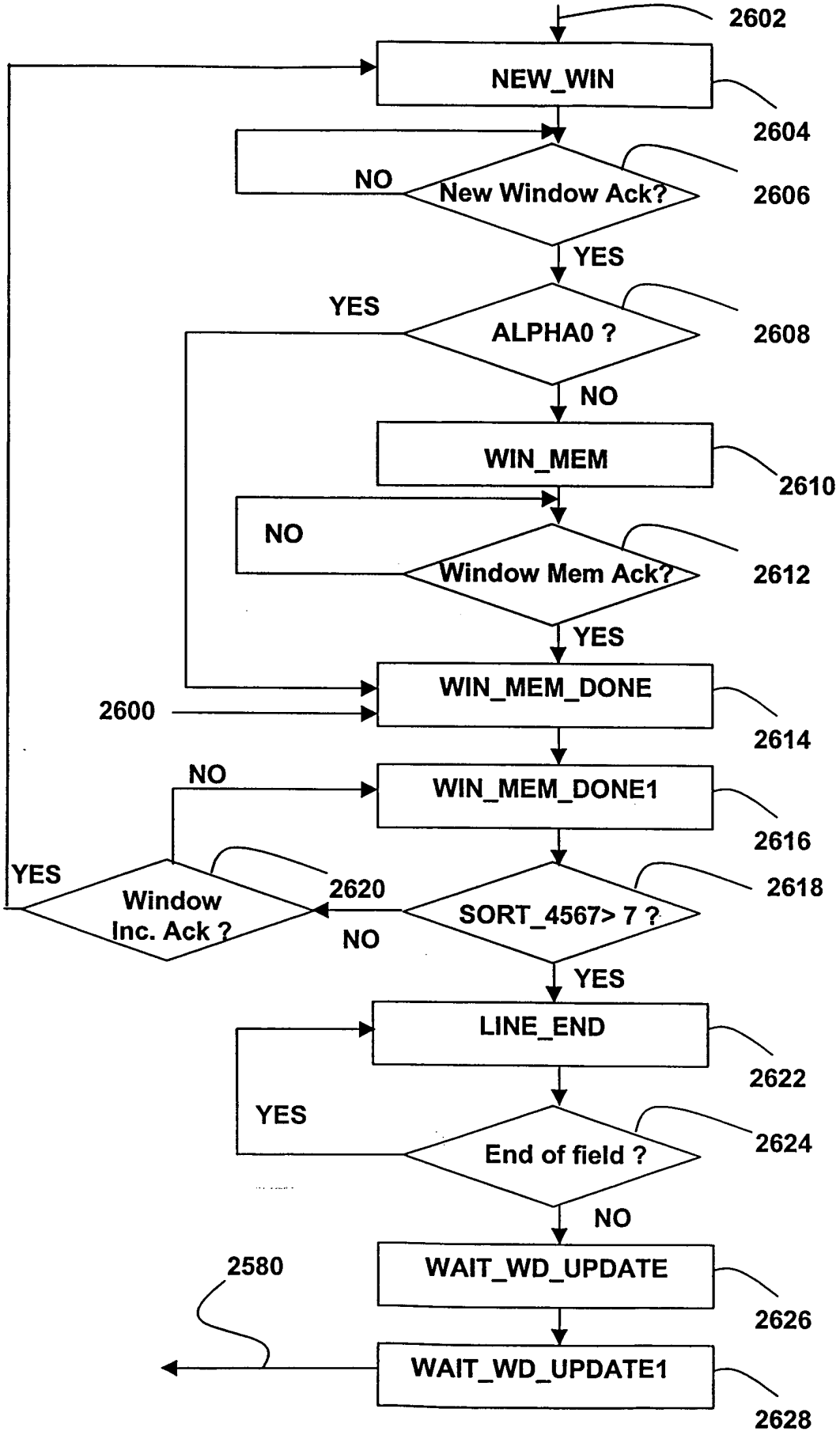
2602
NEW_WIN
2604
NO
New Window Ack?
2606
YES
YES
ALPHA0 ?
2608
NO
WIN_MEM
2610
NO
Window Mem Ack?
2612
YES
WIN_MEM_DONE
2600
2614
NO
WIN_MEM_DONE1
2616
YES
Window Inc. Ack ?
2620
SORT_4567> 7 ?
2618
NO
YES
LINE_END
2622
YES
End of field ?
2624
NO
2580
WAIT_WD_UPDATE
2626
WAIT_WD_UPDATE1
2628

FIG. 67

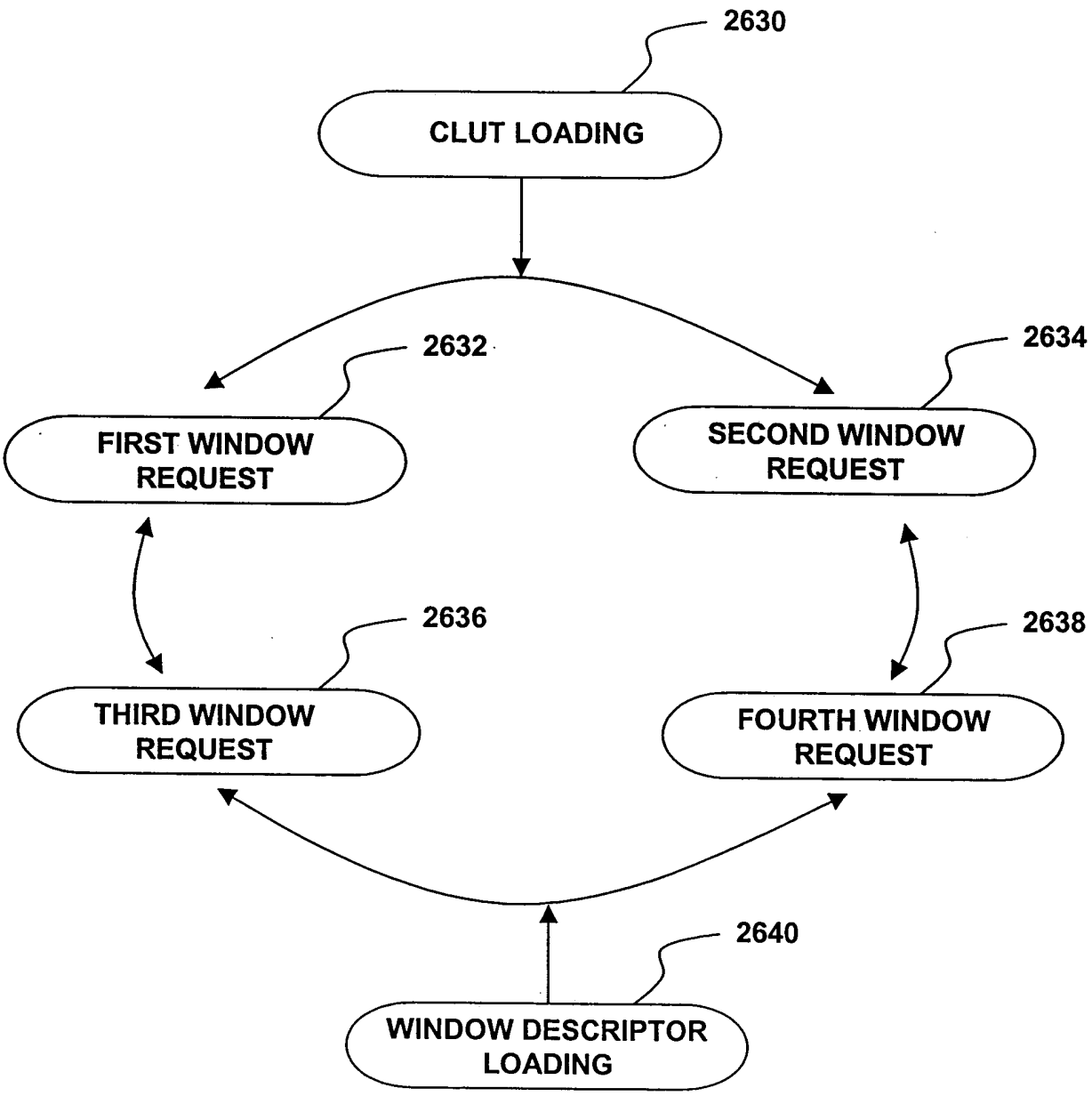
2630
CLUT LOADING
2632
FIRST WINDOW REQUEST
2634
SECOND WINDOW REQUEST
2636
THIRD WINDOW REQUEST
2638
FOURTH WINDOW REQUEST
2640
WINDOW DESCRIPTOR LOADING

FIG. 68

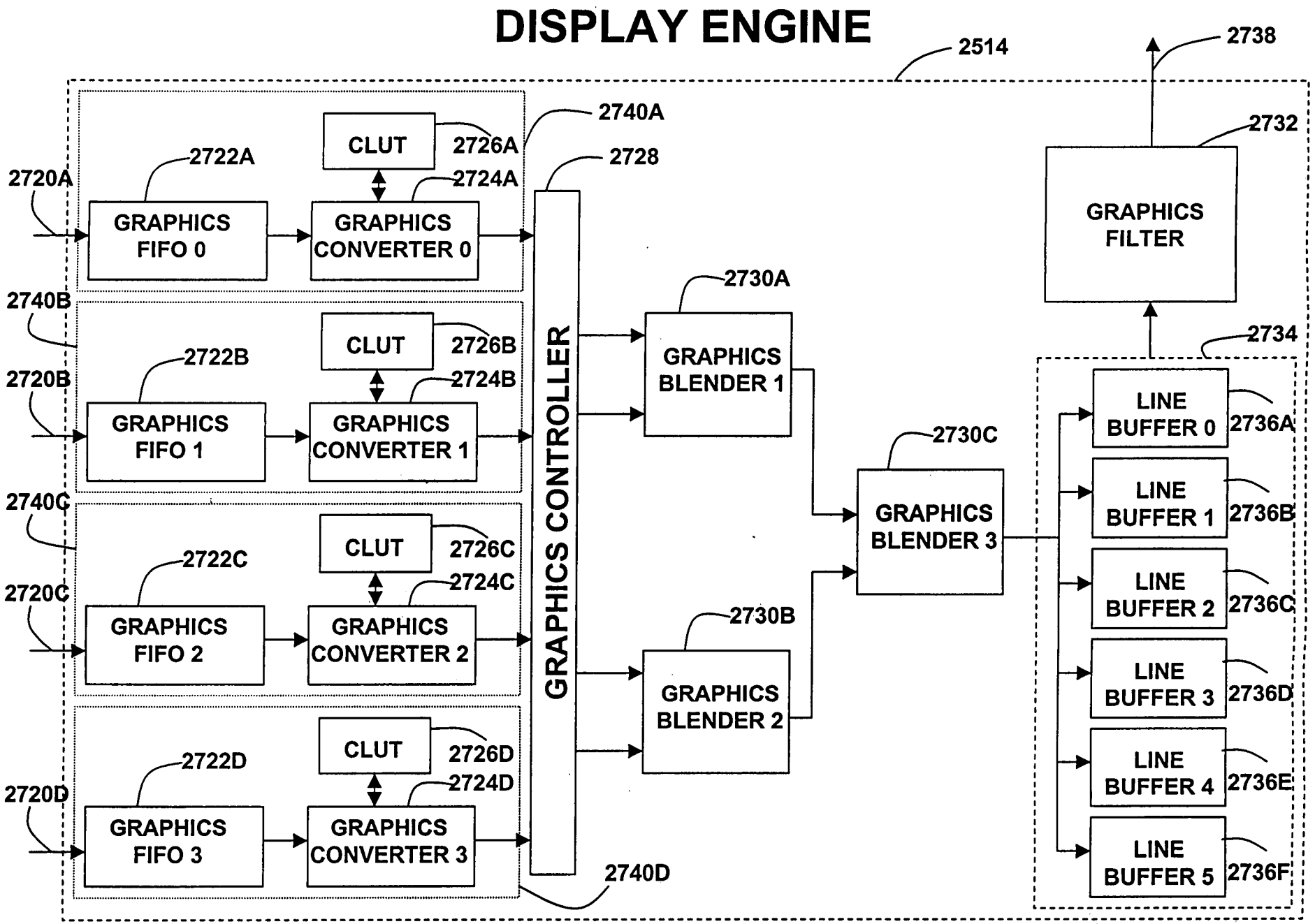
DISPLAY ENGINE
2514
2738
2740A
2728
2732
CLUT
2726A
2722A
2720A
2724A
GRAPHICS FIFO 0
GRAPHICS CONVERTER 0
GRAPHICS FILTER
2740B
2730A
CLUT
2726B
2734
2722B
2720B
2724B
GRAPHICS FIFO 1
GRAPHICS CONVERTER 1
GRAPHICS BLENDER 1
LINE BUFFER 0
2736A
2740C
2730C
CLUT
2726C
LINE BUFFER 1
2736B
2722C
2724C
2720C
GRAPHICS FIFO 2
GRAPHICS CONVERTER 2
GRAPHICS BLENDER 3
LINE BUFFER 2
2736C
GRAPHICS CONTROLLER
2730B
LINE BUFFER 3
2736D
CLUT
2726D
2722D
2724D
2720D
GRAPHICS FIFO 3
GRAPHICS CONVERTER 3
GRAPHICS BLENDER 2
LINE BUFFER 4
2736E
LINE BUFFER 5
2736F
2740D

FIG. 69

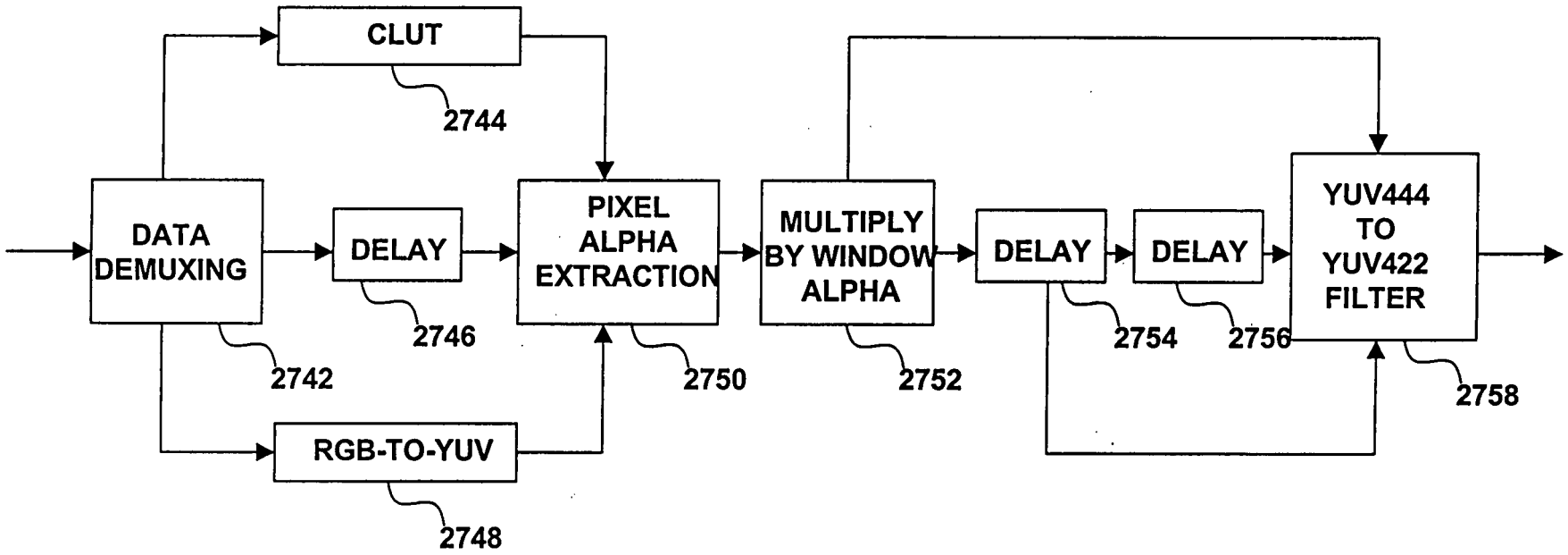
CLUT
2744
DATA DEMUXING
DELAY
2746
PIXEL ALPHA EXTRACTION
MULTIPLY BY WINDOW ALPHA
DELAY
DELAY
YUV444 TO YUV422 FILTER
2742
2750
2752
2754
2756
2758
RGB-TO-YUV
2748

FIG. 70

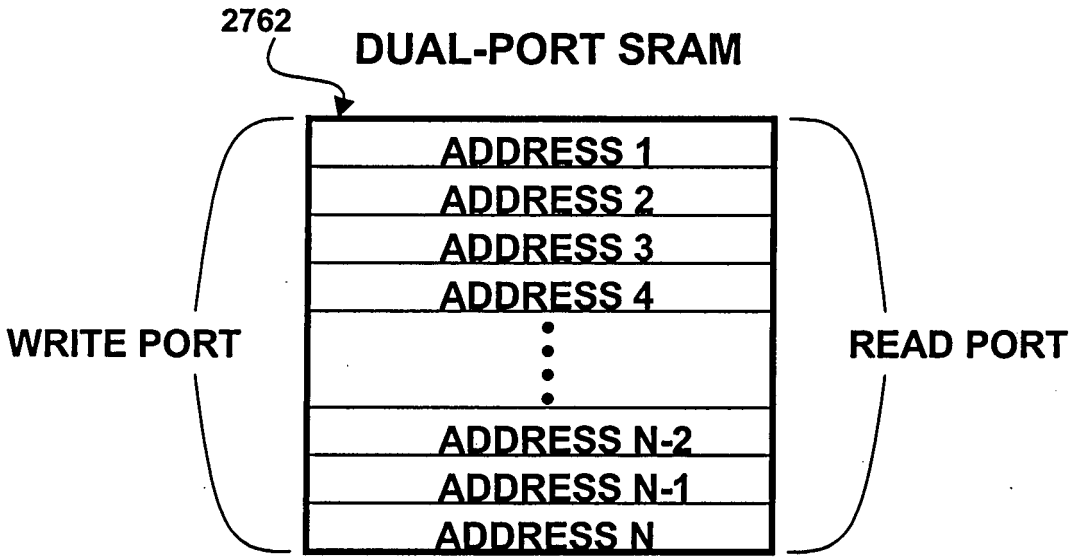
2762
DUAL-PORT SRAM
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS 4
ADDRESS N-2
ADDRESS N-1
ADDRESS N
WRITE PORT
READ PORT

FIG. 71

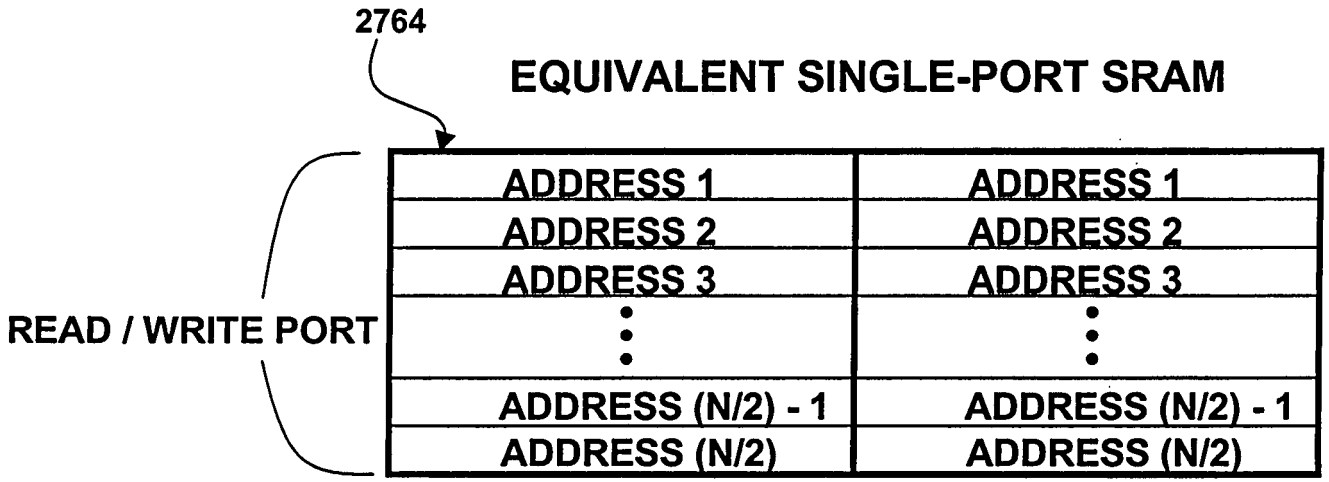
2764
EQUIVALENT SINGLE-PORT SRAM
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS (N/2) - 1
ADDRESS (N/2)
ADDRESS 1
ADDRESS 2
ADDRESS 3
ADDRESS (N/2) - 1
ADDRESS (N/2)
READ / WRITE PORT

FIG. 72

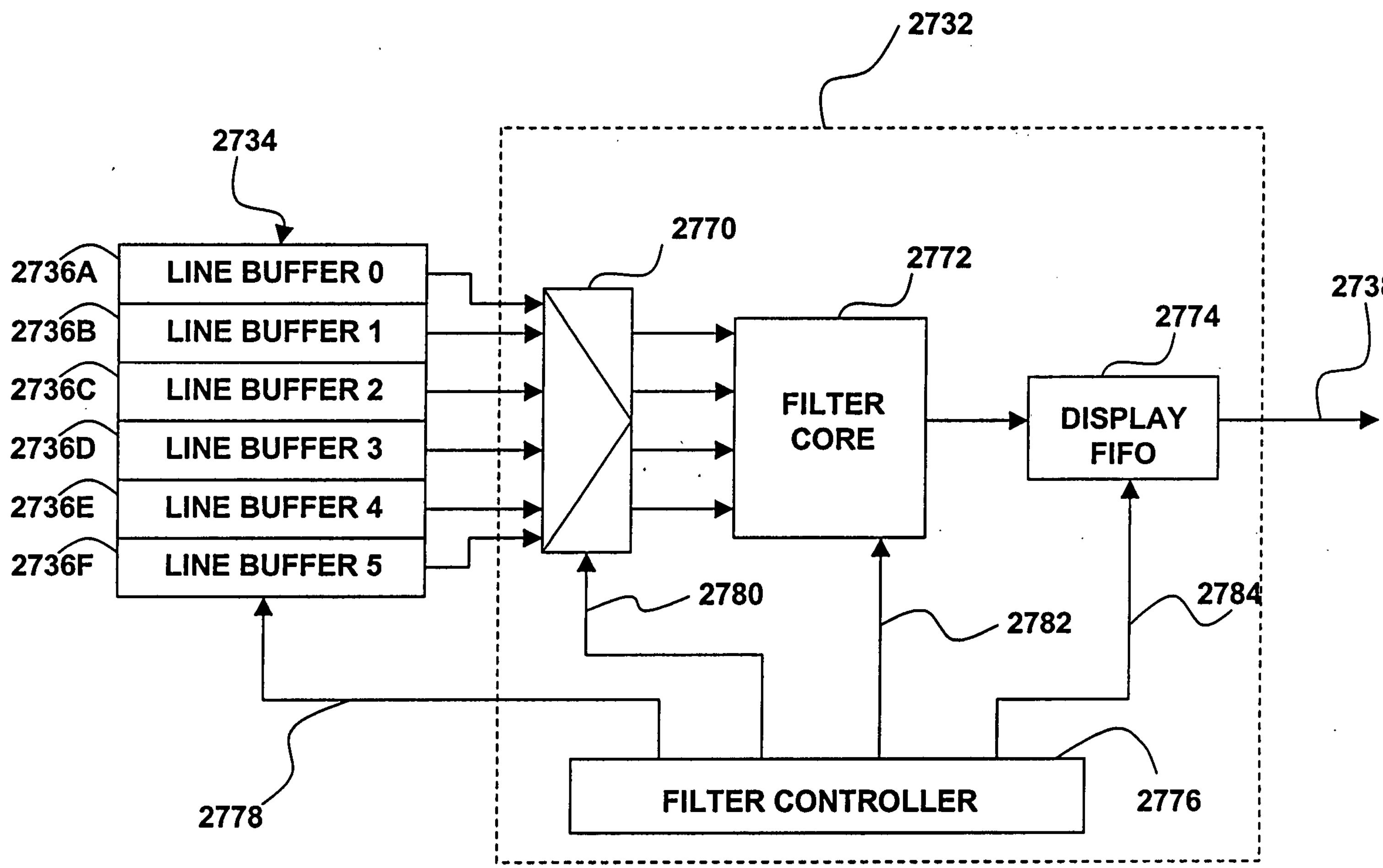
2732
2734
2736A
2736B
2736C
2736D
2736E
2736F
LINE BUFFER 0
LINE BUFFER 1
LINE BUFFER 2
LINE BUFFER 3
LINE BUFFER 4
LINE BUFFER 5
2770
2772
FILTER CORE
2774
DISPLAY FIFO
2738
2780
2782
2784
2778
FILTER CONTROLLER
2776

FIG. 73

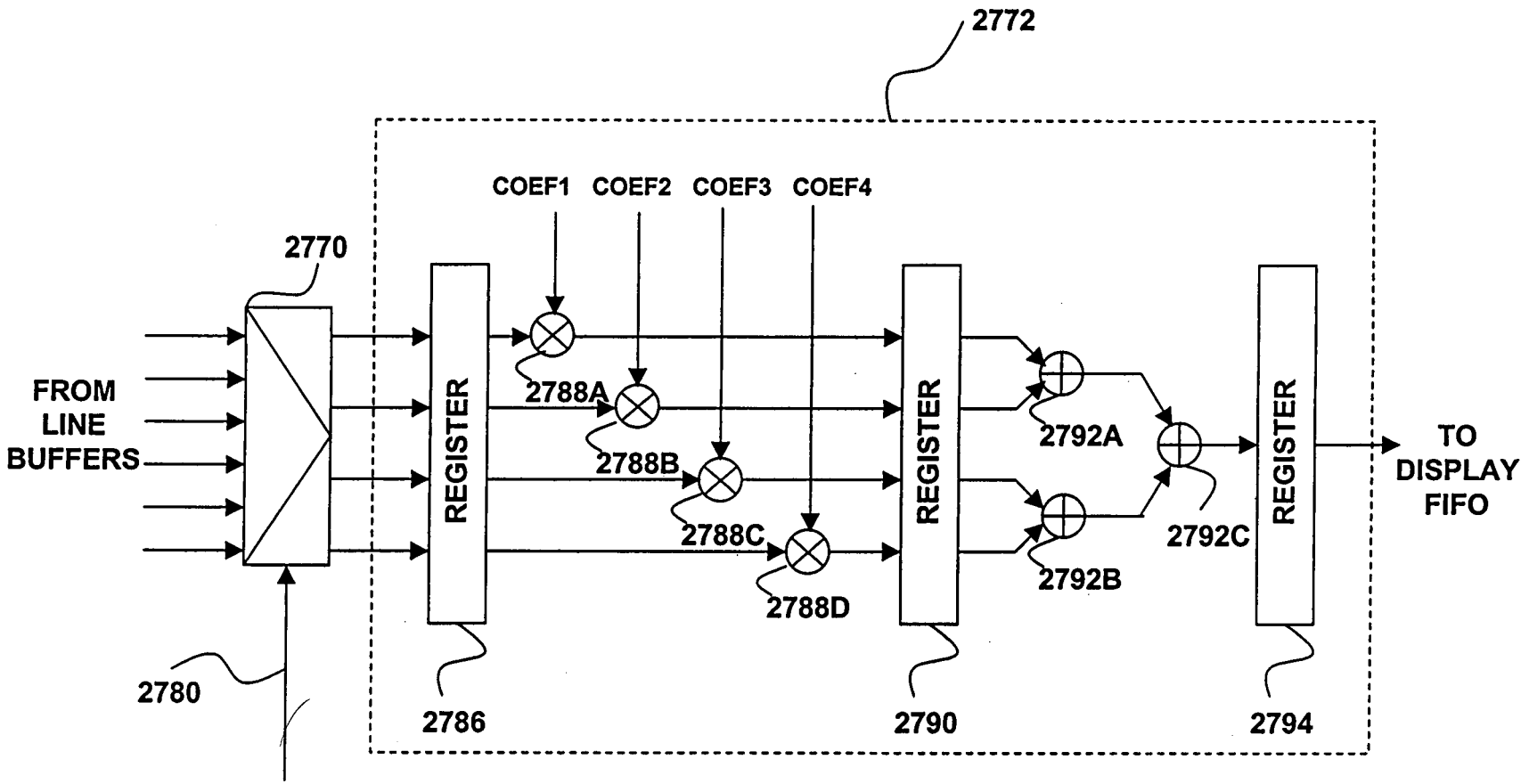

FIG. 74